

Wright State University

CORE Scholar

---

[Browse all Theses and Dissertations](#)

[Theses and Dissertations](#)

---

2010

## Relative Stability of the Inner-Current Loop of Peak Current-Mode Controlled PWM DC-DC Converters in CCM

Nisha Kondrath  
*Wright State University*

Follow this and additional works at: [https://corescholar.libraries.wright.edu/etd\\_all](https://corescholar.libraries.wright.edu/etd_all)



Part of the [Engineering Commons](#)

---

### Repository Citation

Kondrath, Nisha, "Relative Stability of the Inner-Current Loop of Peak Current-Mode Controlled PWM DC-DC Converters in CCM" (2010). *Browse all Theses and Dissertations*. 998.  
[https://corescholar.libraries.wright.edu/etd\\_all/998](https://corescholar.libraries.wright.edu/etd_all/998)

This Dissertation is brought to you for free and open access by the Theses and Dissertations at CORE Scholar. It has been accepted for inclusion in Browse all Theses and Dissertations by an authorized administrator of CORE Scholar. For more information, please contact [library-corescholar@wright.edu](mailto:library-corescholar@wright.edu).

# **RELATIVE STABILITY OF THE INNER-CURRENT LOOP IN PEAK CURRENT-MODE CONTROLLED PWM DC-DC CONVERTERS IN CCM**

A dissertation submitted in partial fulfillment  
of the requirements for the degree of  
**Doctor of Philosophy**

By

**Nisha Kondrath**

B. Tech., Mahatma Gandhi University, Kerala, India, 2002

M. S., Wright State University, Dayton, Ohio, 2005

---

2010  
**Wright State University**

WRIGHT STATE UNIVERSITY  
SCHOOL OF GRADUATE STUDIES

June 15, 2010

I HEREBY RECOMMEND THAT THE DISSERTATION PREPARED UNDER MY SUPERVISION BY Nisha Kondrath ENTITLED Relative Stability of the Inner-Current Loop of Peak Current-Mode Controlled PWM DC-DC Converters in CCM BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Doctor of Philosophy.

---

Marian K. Kazimierczuk, Ph.D.  
Dissertation Director

---

Ramana V. Grandhi, Ph.D.  
Director, Ph.D. in Engineering Program

---

John A. Bantle, Ph.D.  
Vice President for Research and Graduate Studies,  
Interim Dean, School of Graduate Studies

Committee on  
Final Examination

---

Marian K. Kazimierczuk, Ph.D.

---

Raymond E. Siferd, Ph.D.

---

Kuldip S. Rattan, Ph.D.

---

Malcolm W. Daniels, Ph.D.

---

Brad Bryant, Ph.D.

## Abstract

Kondrath, Nisha. Ph.D., Engineering Ph.D. Program, Wright State University, 2010. *Relative Stability of the Inner-Current Loop in Peak Current-Mode Controlled PWM DC-DC Converters in CCM.*

Current-mode control is a commonly adopted method of regulation for pulse-width modulated (PWM) dc-dc power converters in industry, but is not well understood. The advantages of current-mode control over the voltage-mode control include inherent overload and short circuit protection, faster response, line-noise rejection, and multiple converter paralleling. Current-mode controlled system consists of (1) an inner-current loop and (2) an outer-voltage loop, which sets the reference voltage to the inner loop. To ensure stable operation of the multi-loop converter, all the sequential loops in the circuit should be stable with sufficient degree of stability. The research in this dissertation is focused on the relative stability of the inner-current loop in peak current-mode (PCM) controlled PWM dc-dc converters operating in CCM.

The operating principle of peak current-mode control is presented. The inner-current loop dynamics of a peak current-mode controlled dc-dc converter is investigated using perturbation theory. Considering its mixed-signal (analog and digital) behavior, the current loop is modeled using sample-and-hold theory. Taking the discrete nature of the inner-current loop into account, a closed-loop transfer function for the current loop is derived in z-domain and an equivalent-hold approximation is used to derive an approximate closed-loop transfer function in the continuous s-domain using modified Padé approximation. A general expression for the loop gain of the inner-loop, independent of the converter topology, is derived. Using the loop gain, a measure of relative stability of the inner loop is developed. Expressions for amount of slope compensation required at maximum duty cycle, for the inner loop to be



marginally stable and to achieve a specified margin of stability, are derived. Also, expressions for maximum duty cycle at a given amount of slope compensation, for the inner loop to be marginally stable and to obtain a specified margin of stability, are derived. The control current expressions for the inner loop of peak current-mode controlled converters without and with slope compensation are derived. A procedure to design the inner-current loop is developed. Saber Sketch simulation and experimental results are presented to validate the presented theory.

The dynamic behavior of the inner-current loop of peak current-mode controlled PWM dc-dc buck converter operating in CCM is analyzed. The critical path power stage transfer functions, the relevant inner-current loop transfer functions, and the control-to-output transfer function of peak current-mode controlled PWM dc-dc buck converter operating in CCM are derived. The presented model is validated using experimental Bode plots.

# Contents

<b>1</b>	<b>Introduction</b>	<b>1</b>
1.1	Background . . . . .	1
1.2	Objectives . . . . .	5
<b>2</b>	<b>Peak Current-Mode Control</b>	<b>7</b>
2.1	Principle of Operation . . . . .	7
2.2	Perturbation Ratio and Perturbation Coefficient . . . . .	9
2.2.1	Stability Analysis . . . . .	10
2.2.2	Current-Mode Control Without Slope Compensation . . . . .	11
2.2.3	Current-Mode Control With Slope Compensation . . . . .	13
2.3	Analysis of Inner-Current Loop Dynamics . . . . .	15
2.4	Sample-and-Hold Modeling . . . . .	17
2.5	Discrete Closed-Loop Transfer Function $H_{icl}(z)$ . . . . .	18
2.6	Closed-Loop Control Voltage-to-Inductor Current Transfer Function $H_{icl}(s)$ . . . . .	21
2.6.1	Comparison of the Actual Function $e^{sT_s}$ and the Approximations	22
2.6.2	Comparison of the Actual Function $H_{icl}(s)$ and the Approximations . . . . .	25
2.6.3	Closed Inner-Current Loop Transfer Function $H_{icl}(s)$ . . . . .	29
2.6.4	Experimental Results . . . . .	29
<b>3</b>	<b>Loop Gain of Inner-Current Loop</b>	<b>33</b>
3.1	Structure of the Inner-Current Loop . . . . .	33
3.2	General Expression for Loop Gain of Inner-Current Loop . . . . .	33
3.3	Margins of Stability . . . . .	35
3.4	Perturbation Ratio $a$ versus Phase Margin $PM$ . . . . .	36

<b>4</b>	<b>Peak Current-Mode Control without Slope Compensation</b>	<b>40</b>
4.1	Boundary Between Stable and Unstable Operations . . . . .	40
4.2	Relative Stability . . . . .	41
4.3	General Equation for Control Current Level . . . . .	42
4.3.1	Buck Converter . . . . .	43
4.3.2	Boost Converter . . . . .	45
4.3.3	Buck-Boost Converter . . . . .	45
4.4	Design Example . . . . .	49
4.5	Simulation Results . . . . .	50
4.6	Experimental Results . . . . .	50
<b>5</b>	<b>Peak Current-Mode Control with Slope Compensation</b>	<b>59</b>
5.1	Boundary Between Stable and Unstable Regions of Operation . . . .	59
5.1.1	Buck and Buck-Boost Converters . . . . .	60
5.1.2	Boost Converter . . . . .	62
5.2	Relative Stability . . . . .	62
5.2.1	Buck and Buck-Boost Converters . . . . .	64
5.2.2	Boost Converter . . . . .	67
5.3	General Equation for Control Current Level with Slope Compensation	67
5.3.1	Buck Converter . . . . .	69
5.3.2	Boost Converter . . . . .	70
5.3.3	Buck-Boost Converter . . . . .	70
5.4	Design Example . . . . .	70
5.4.1	Required Compensation Slope . . . . .	71
5.4.2	Required Control Current . . . . .	72
5.5	Simulation Results . . . . .	72

<b>6</b>	<b>Dynamic Behavior of the Inner-Current Loop of Peak Current-Mode Controlled PWM DC-DC Buck Converter</b>	<b>83</b>
6.1	Small-Signal Model of Buck Converter . . . . .	83
6.2	Duty Ratio-to-Inductor Current Transfer Function of Buck Converter	84
6.2.1	Wide-Frequency Transfer Function . . . . .	85
6.2.2	Low-Frequency Transfer Function . . . . .	86
6.2.3	High-Frequency Transfer Function . . . . .	86
6.2.4	Simulation Results . . . . .	87
6.2.5	Experimental Results . . . . .	87
6.3	Duty Ratio-to-Output Voltage Transfer Function of Buck Converter .	91
6.3.1	Transfer Function . . . . .	91
6.3.2	Simulation Results . . . . .	91
6.3.3	Experimental Results . . . . .	93
6.4	Block Diagram of Current-Mode Controlled Converters with Inner-Current Loop only . . . . .	93
6.5	Closed-Loop Control-to-Inductor Current Transfer Function . . . . .	95
6.6	Loop Gain of the Inner-Current Loop . . . . .	96
6.6.1	Simulation Results . . . . .	96
6.7	Error Voltage-to-Duty Cycle Transfer Function of PCM Controlled Buck Converter . . . . .	98
6.8	Control Voltage-to-Duty Cycle Transfer Function of PCM Controlled Buck Converter . . . . .	98
6.9	Control-to-Output Transfer Function of PCM Controlled Buck Converter	98
6.9.1	Using the Existing Block Diagram . . . . .	101
6.9.2	Using the Proposed Block Diagram . . . . .	101
6.9.3	Simulation Results . . . . .	101
6.9.4	Experimental Results . . . . .	103

<b>7</b>	<b>Conclusions</b>	<b>105</b>
7.1	Summary . . . . .	105
7.2	Contributions . . . . .	106
	<b>Bibliography</b>	<b>108</b>

## List of Figures

1.1	Inner-current loop structure proposed in [12]. . . . .	3
1.2	Inner-current loop structure proposed in [19]. . . . .	3
2.1	PWM dc-dc buck converter with peak current-mode control. . . . .	8
2.2	Relevant waveforms in the inner-current loop of peak current-mode controlled PWM dc-dc converter. . . . .	8
2.3	Steady-state (solid line) and perturbed (dashed line) inductor current waveforms. (a) Stable system, $a < 1$ . (b) Marginally stable system, $a = 1$ . (c) Unstable system, $a > 1$ . . . . .	12
2.4	Steady-state (solid-line) and perturbed (dashed-line) waveforms of the inductor current for current-mode control without slope compensation. . . . .	13
2.5	Steady-state (solid-line) and perturbed (dashed-line) waveforms of the inductor current for current-mode control with slope compensation. . . . .	14
2.6	Peak current-mode controlled dc-dc buck converter with inner-current loop only. . . . .	15
2.7	Waveforms describing the inner-current loop dynamics . . . . .	16
2.8	Block diagram of inner-current loop. . . . .	17
2.9	Steady state (solid line) and perturbed (dashed line) inductor current $i_L$ and control current $i_C, i_C - i_A$ waveforms. . . . .	18
2.10	Position of the z-domain closed-loop pole $a$ in the unit circle for stable, marginally stable, and unstable inner loop. . . . .	21
2.11	Comparison of the actual function $e^{sT_s}$ , the first, second and third-order Padé approximations. (a) Semilog scale. (b) Linear scale. . . . .	23
2.12	Comparison of the actual function $e^{sT_s}$ , the second order Padé approximation, and the second order modified Padé approximations. (a) Semilog scale. (b) Linear scale. . . . .	24

2.13	Comparison of Bode plots of the actual function $H_{icl}(s)$ , the second-order Padé approximation, and the second-order modified Padé approximation at $a = 0.2$ . (a) Magnitude. (b) Phase. . . . .	26
2.14	Comparison of enlarged Bode plots of the actual function $H_{icl}(s)$ , the second-order Padé approximation, and the second-order modified Padé approximation at $a = 0.2$ . (a) Magnitude. (b) Phase. . . . .	27
2.15	Comparison of the actual function $H_{icl}(s)$ , the second-order Padé approximation, and the second-order modified Padé approximation in a linear scale at $a = 0.2$ . (a) Magnitude. (b) Phase. . . . .	28
2.16	Bode plots of the closed-loop gain $H_{icl}(s)$ at $a = 0.29$ , $a = 0.5$ , and $a = 0.95$ . (a) Magnitude. (b) Phase. . . . .	30
2.17	Experimental Bode plots of the closed-loop gain $H_{icl}(s)$ at $a = 0.29$ , $a = 0.5$ , and $a = 0.95$ . . . . .	32
3.1	Closed-loop structure of the inner-current loop for ac components. . .	33
3.2	Bode plots of the loop gain $T_i(s)$ at $a = 0.1237$ and $a = 0.9$ . . . . .	34
3.3	Normalized cross-over frequency $f_{ci}/f_s$ as a function of perturbation ratio $a$ . . . . .	38
3.4	Perturbation ratio $a$ versus phase margin $PM$ . . . . .	39
4.1	Phase margin $PM$ as a function of duty cycle $D$ for peak current-mode control without compensation. . . . .	41
4.2	Steady-state inductor current $i_L$ waveform and control current $I_{CN}$ without slope compensation. . . . .	42
4.3	DC control current $I_{CN}$ as functions of duty cycle $D$ and phase margin $PM$ for buck converter with $V_O = 7$ V, $I_O = 0.7$ A, $L = 254$ $\mu$ H, and $f_s = 100$ kHz. (a) $I_{CN}$ versus $D$ . (b) $I_{CN}$ versus $PM$ . . . . .	44

4.4	DC control current $I_{CN}$ as functions of duty cycle $D$ and phase margin $PM$ for boost converter with $V_O = 400$ V, $I_O = 0.225$ A, $L = 20$ mH, and $f_s = 100$ kHz. (a) $I_{CN}$ versus $D$ . (b) $I_{CN}$ versus $PM$ . . . . .	46
4.5	DC control current $I_{CN}$ as functions of duty cycle $D$ and phase margin $PM$ for buck-boost converter with $V_O = 28$ V, $I_O = 2$ A, $L = 334$ $\mu$ H, and $f_s = 100$ kHz. (a) $I_{CN}$ versus $D$ . (b) $I_{CN}$ versus $PM$ . . . . .	47
4.6	Peak current-mode controlled PWM dc-dc buck converter with inner-current loop only. . . . .	48
4.7	Control voltage $V_{CN}$ , sensed inductor current $R_s i_L$ , and MOSFET gate-to-source voltage $V_{GS}$ waveforms obtained using Saber simulations. (a) $V_I = 35$ V and $V_{CN} = R_s I_{CN} = 0.8102$ V. (b) $V_I = 20$ V and $V_{CN} = R_s I_{CN} = 0.7896$ V. . . . .	51
4.8	Control voltage $V_{CN}$ , sensed inductor current $R_s i_L$ , and MOSFET gate-to-source voltage $V_{GS}$ waveforms obtained using Saber simulations. (a) $V_I = 14$ V and $V_{CN} = R_s I_{CN} = 0.7689$ V. (b) $V_I = 12$ V and $V_{CN} = R_s I_{CN} = 0.7689$ V. . . . .	52
4.9	Comparison of theoretical and Saber simulation results. . . . .	53
4.10	Experimental setup to measure duty cycle at given values of control voltage. . . . .	54
4.11	Experimental and theoretical values of DC control current $I_{CN}$ as functions of duty cycle $D$ and input voltage $V_I$ for buck converter with $V_O = 7$ V, $I_O = 0.7$ A, $L = 254$ $\mu$ H, $f_s = 100$ kHz, and $R_s = 1$ $\Omega$ . (a) $I_{CN}$ versus $D$ . (b) $I_{CN}$ versus $V_I$ . . . . .	55
4.12	Sensed inductor ripple current $R_s(i_L - I_L)$ and MOSFET gate-to-source $V_{GS}$ voltage waveforms from the experimental set-up with $V_I = 35$ V and $V_{CN} = R_s I_{CN} = 0.81$ V. . . . .	56



4.13	Sensed inductor ripple current $R_s(i_L - I_L)$ and MOSFET gate-to-source voltage waveforms from the experimental set-up with $V_I = 20$ V and $V_{CN} = R_s I_{CN} = 0.79$ V. . . . .	56
4.14	Sensed inductor ripple current $R_s(i_L - I_L)$ and MOSFET gate-to-source voltage $V_{GS}$ waveforms from the experimental set-up with $V_I = 15.56$ V and $V_{CN} = R_s I_{CN} = 0.776$ V. . . . .	57
4.15	Sensed inductor ripple current $R_s(i_L - I_L)$ and MOSFET gate-to-source voltage $V_{GS}$ waveforms showing transformation from stable to unstable operation. (a) $V_I = 15$ V and $V_{CN} = R_s I_{CN} = 0.769$ V. (b) $V_I = 14$ V and $V_{CN} = R_s I_{CN} = 0.769$ V. (c) $V_I = 12.56$ V and $V_{CN} = R_s I_{CN} = 0.769$ V. . . . .	58
5.1	Boundary between stable and unstable regions of operations for buck and buck-boost converters. (a) $M_{3cr}/(V_O/L)$ versus $D_{max}$ . (b) $D_{lim}$ versus $M_3/(V_O/L)$ . . . . .	61
5.2	Boundary between stable and unstable regions of operations for boost converter. (a) $M_{3cr}/(V_O/L)$ versus $D_{max}$ . (b) $D_{lim}$ versus $M_3/(V_O/L)$ . . . . .	63
5.3	Minimum value of required compensation slope to achieve a specified phase margin for buck and buck-boost converters. (a) $M_{3min}/(V_O/L)$ versus $D_{max}$ . (b) $D_{max}$ versus $M_3/(V_O/L)$ . . . . .	66
5.4	Minimum value of required compensation slope to achieve a specified phase margin for boost converter. (a) $M_{3min}/(V_O/L)$ versus $D_{max}$ . (b) $D_{max}$ versus $M_3/(V_O/L)$ . . . . .	68
5.5	Steady-state inductor current $i_L$ waveform and control current $I_{CS}$ with slope compensation. . . . .	69
5.6	Comparison of theoretical and Saber simulation results. . . . .	74

5.7	Control voltage $V_{CS}$ , compensating ramp $v_A$ , sensed inductor current $R_s i_L$ , and MOSFET gate-to-source voltage $V_{GS}$ waveforms obtained using Saber simulations at $PM = 60^\circ$ . (a) $V_I = 16$ V and $V_{CS} = R_s I_{CS} = 1.561$ V. (b) $V_I = 20$ V and $V_{CN} = R_s I_{CS} = 1.536$ V. . . . .	75
5.8	Control voltage $V_{CS}$ , compensating ramp $v_A$ , sensed inductor current $R_s i_L$ , and MOSFET gate-to-source voltage $V_{GS}$ waveforms obtained using Saber simulations at $PM = 60^\circ$ . (a) $V_I = 24$ V and $V_{CS} = R_s I_{CS} = 1.52$ V. (b) $V_I = 28$ V and $V_{CN} = R_s I_{CS} = 1.508$ V. . . . .	76
5.9	Control voltage $V_{CS}$ , compensating ramp $v_A$ , sensed inductor current $R_s i_L$ , and MOSFET gate-to-source voltage $V_{GS}$ waveforms obtained using Saber simulations at $PM = 45^\circ$ . (a) $V_I = 16$ V and $V_{CS} = R_s I_{CS} = 1.504$ V. (b) $V_I = 20$ V and $V_{CN} = R_s I_{CS} = 1.549$ V. . . . .	77
5.10	Control voltage $V_{CS}$ , compensating ramp $v_A$ , sensed inductor current $R_s i_L$ , and MOSFET gate-to-source voltage $V_{GS}$ waveforms obtained using Saber simulations at $PM = 45^\circ$ . (a) $V_I = 24$ V and $V_{CS} = R_s I_{CS} = 1.481$ V. (b) $V_I = 28$ V and $V_{CN} = R_s I_{CS} = 1.475$ V. . . . .	78
5.11	Control voltage $V_{CS}$ , compensating ramp $v_A$ , sensed inductor current $R_s i_L$ , and MOSFET gate-to-source voltage $V_{GS}$ waveforms obtained using Saber simulations at $PM = 30^\circ$ . (a) $V_I = 16$ V and $V_{CS} = R_s I_{CS} = 1.458$ V. (b) $V_I = 20$ V and $V_{CN} = R_s I_{CS} = 1.454$ V. . . . .	79
5.12	Control voltage $V_{CS}$ , compensating ramp $v_A$ , sensed inductor current $R_s i_L$ , and MOSFET gate-to-source voltage $V_{GS}$ waveforms obtained using Saber simulations at $PM = 30^\circ$ . (a) $V_I = 24$ V and $V_{CS} = R_s I_{CS} = 1.451$ V. (b) $V_I = 28$ V and $V_{CN} = R_s I_{CS} = 1.449$ V. . . . .	80

5.13	Control voltage $V_{CS}$ , compensating ramp $v_A$ , sensed inductor current $R_s i_L$ , and MOSFET gate-to-source voltage $V_{GS}$ waveforms obtained using Saber simulations at $PM = 0^\circ$ . (a) $V_I = 16$ V and $V_{CS} = R_s I_{CS} = 1.377$ V. (b) $V_I = 20$ V and $V_{CN} = R_s I_{CS} = 1.389$ V. . . . .	81
5.14	Control voltage $V_{CS}$ , compensating ramp $v_A$ , sensed inductor current $R_s i_L$ , and MOSFET gate-to-source voltage $V_{GS}$ waveforms obtained using Saber simulations at $PM = 0^\circ$ . (a) $V_I = 24$ V and $V_{CS} = R_s I_{CS} = 1.397$ V. (b) $V_I = 28$ V and $V_{CN} = R_s I_{CS} = 1.402$ V. . . . .	82
6.1	Open-loop PWM dc-dc buck converter. (a) Circuit. (b) Small-signal model. . . . .	84
6.2	Small-signal model of a buck converter to derive duty cycle-to-inductor current and duty cycle-to-output voltage transfer functions. . . . .	85
6.3	Magnitude plots of duty cycle-to-inductor current transfer function at given input voltages. (a) Wide-frequency plots. (b) High-frequency plots. . . . .	88
6.4	Phase plots of duty cycle-to-inductor current transfer function. . . . .	89
6.5	Experimental Bode plots of duty cycle-to-inductor current transfer function from Hewlett-Packard 4194A Impedance/Gain-Phase Analyzer. . . . .	90
6.6	Bode plots of duty cycle-to-output voltage transfer function at given input voltages. (a) Magnitude. (b) Phase. . . . .	92
6.7	Experimental Bode plots of duty cycle-to-output voltage transfer function from Hewlett-Packard 4194A Impedance/Gain-Phase Analyzer. . . . .	94
6.8	Block diagrams to determine control-to-output transfer function. . . . .	95
6.9	Bode plots of loop gain $T_i(s)$ of the inner-current loop at given values of $a$ . (a) Magnitude. (b) Phase. . . . .	97
6.10	Bode plots of error voltage-to-duty cycle $T_{ms}(s)$ transfer function at given values of $a$ . (a) Magnitude. (b) Phase. . . . .	99

6.11	Bode plots of control voltage-to-duty cycle transfer function $T_{icl}(s)$ at given values of $a$ . (a) Magnitude. (b) Phase. . . . .	100
6.12	Bode plots of control-to-output transfer function $T_{co}(s)$ at given values of $a$ . (a) Magnitude. (b) Phase. . . . .	102
6.13	Experimental Bode plots of control voltage-to-output voltage transfer function from Hewlett-Packard 4194A Impedance/Gain-Phase Analyzer.	104

## List of Tables

2.1	$V_I$ , $D$ , $V_C$ , and $a$ used in the experimental measurement. . . . .	31
4.1	$I_{CN}$ and $V_{CN}$ required at specified values of $V_I$ and $R_s = 1 \Omega$ to obtain $V_O = 7 \text{ V}$ . . . . .	49
5.1	Minimum compensation slope $M_{3min}$ and amplitude of the compensation ramp to obtain $D_{max} = 0.75$ at given values of $PM$ . . . . .	72
5.2	Minimum compensation slope $M_{3min}$ and control current to obtain $D_{max} = 0.75$ at given values of $PM$ and duty cycle $D$ . . . . .	73
6.1	Corner frequencies and dc gains of $T_{pi}(s)$ at given values of input voltage. . . . .	87
6.2	Corner frequencies and dc gains of $T_p(s)$ at given values of input voltage. . . . .	93
6.3	Cross-over frequencies and phase margins of $T_i(s)$ at given values of input voltage. . . . .	96
6.4	Cross-over frequencies and phase values of $T_{co}(s)$ at given values of input voltage. . . . .	103

## Acknowledgements

I would like to thank my advisor, Dr. Marian K. Kazimierczuk, for his academic guidance and support for the duration of the Ph.D. program. I am grateful for his mentoring, advice, and research support.

I also wish to thank Dr. Raymond Siferd, Dr. Kuldip Rattan, Dr. Malcolm Daniels, and Dr. Brad Bryant for serving as members of my Ph.D. defense committee. I would like to extend my gratitude to the committee members for their advice and constructive criticism. I also want to thank the Ph.D. program and the Department of Electrical Engineering at Wright State University for giving me the opportunity to obtain my Ph.D. degree at Wright State University.

A special thanks goes to my loving husband, for his patience, love, support, and encouragement through these years.

# 1 Introduction

## 1.1 Background

Current-mode control is a commonly adopted method of regulation for pulse-width modulated (PWM) dc-dc converters, but not well studied or understood. The advantages of current-mode control over the voltage-mode control includes better overload and short circuit protection, multiple converter paralleling, line-noise rejection, and design flexibility [1]-[33]. There are different types of current-mode control techniques available such as *constant-frequency control* and *variable-frequency control*. The constant-frequency current-mode control includes *peak current-mode control*, *valley current-mode control*, and *average current-mode control*. The variable-frequency current-mode control includes *constant on-time control* and *constant off-time control*. This work analyzes the behavior of constant frequency peak current-mode controlled PWM dc-dc converters operating in continuous-conduction mode (CCM).

Current-mode controlled converters consist of two loops: an inner-current loop and an outer-voltage loop. The inner-current loop directly controls the inductor current, which is a function of the output current in dc-dc converters, and supplies the duty cycle of the converter. Therefore, the inner-loop indirectly controls the output voltage. The outer-voltage loop directly controls the output voltage and supplies the required control voltage for the inner-current loop. This research focuses on the analysis of the inner-current loop of peak current-mode controlled dc-dc converters. The inner-current loop usually consists of a sense resistor, a comparator, and a R-S flip-flop. A current transformer or a current probe could be used instead of a sense resistor [42]-[43].

For a system to be stable, it is necessary to have all the successive loops be stable [7]. To ensure a stable operation of the system, each successive loop should be stable with sufficient degree of stability. Therefore, in a current-mode controlled system, it

has to be ensured that the inner-current loop is stable with sufficient margin from the boundary. Several different approaches to modeling current-mode control are available in the literature [12], [18], [19], [28]. It has been proposed that current-mode control transforms the power stage into a current source which supplies the load [7], [19]. Also, it is believed that the power stage reduces into an inductor, even though it is only true in the high-frequency range. The sample and hold modeling of the inner-current loop was first presented in [11] and had used discrete domain transfer functions to model the current-mode control. Using equivalent hold modeling proposed in [11], two different models for the inner-current loop were introduced in [12] and [19].

The inner-current loop model presented in [12] is shown in Fig. 1.1.  $F_m$  is the modulator gain,  $k_f$  and  $k_r$  are the feed-forward gains,  $v_{on}$  and  $v_{off}$  are the voltages across the inductor when the MOSFET is on and off, respectively,  $R_i$  is the sense resistance, and  $H_e(s)$  represents the sample and hold part.  $H_e(s)$  is dependent on the first-order power stage transfer function  $F_i(s) = \frac{i_l(s)}{d(s)}$ , which is only valid in the high-frequency range. Also, the power stage transfer function  $F_i(s)$  is a function of  $R_i$ , the sense resistor. An unified modeling of current-mode controlled converters independent of converter topology was done in [19] by introducing new unified input quantities  $v_{off}$  and  $i_{on}$ . Therefore, the realization of the circuitry compatible with the model is harder. Though a stability parameter  $Q_s$  is presented, the paper failed to present any measures of relative stability of the system.

Yet another structure for the inner-current loop was presented in [28], which is adopted in this research. The work in this paper has presented the relationship of perturbations in inductor current at the beginning and at the end of a cycle,  $a = \frac{\Delta i_{l(k+1)}}{\Delta i_{l(k)}}$ , to the phase margin  $PM$ . But,  $a$  is an invisible parameter (not a physical quantity) compared to a design parameter. A measure of relative stability of the inner loop in terms of design parameters is missing. Some of the recent literatures in the



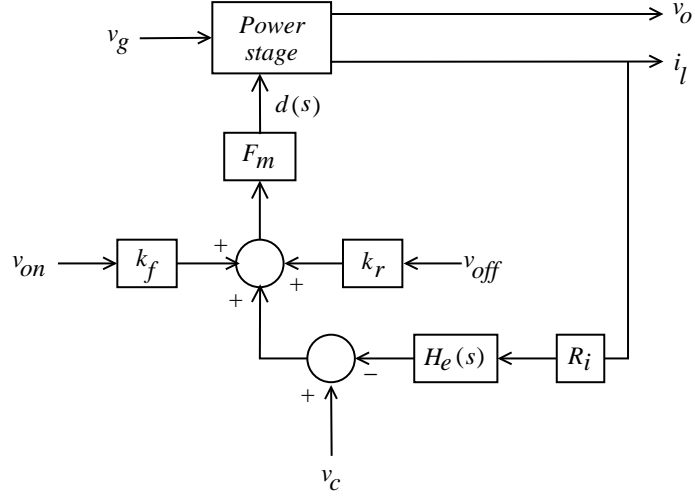


Figure 1.1: Inner-current loop structure proposed in [12].

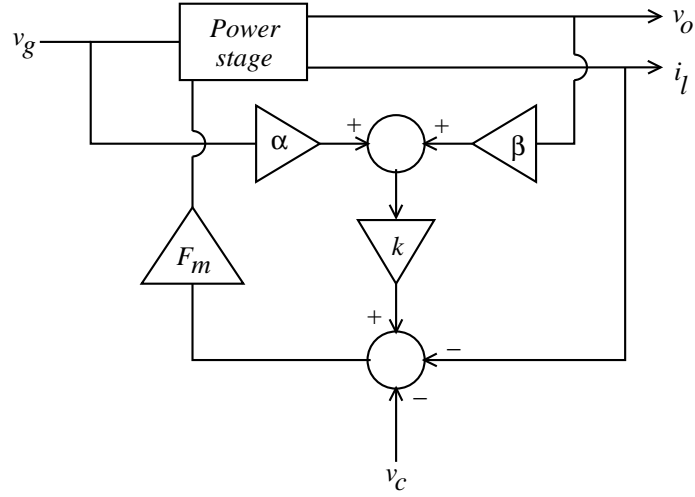


Figure 1.2: Inner-current loop structure proposed in [19].

subject deals with the modeling of average-input current-mode controlled converter [23]. The authors have adopted the approaches presented in [12] and [19] to model the average current-mode control. [30] presented the minimum value of compensating slope required by the inner-loop of current-mode controlled converters to be stable. But any measure of margin of stability seems to be absent.

As already mentioned, to ensure a stable operation of the current-mode controlled converter, each successive loop should be stable with sufficient degree of stability. Any measure of relative stability of the inner loop is absent in the literature thus far. This

research analyzes the relative stability of the inner-current loop of peak current-mode controlled converters. Also, a design procedure for the inner-current loop design to achieve a specified stability margin is absent in the literature. The design of the inner loop consists of three steps:

1. Determination of the required amount of slope compensation, if needed.
2. Calculation of the required control current range to supply the required range of duty cycle.
3. Selection of the value of the sense resistor.

The value of required compensation slope depends on the required margin of stability as well as the maximum duty cycle specified by the converter power stage. The range of control current should be known to select appropriate value of the sense resistance in order to avoid saturation of the op-amp in the outer loop compensator as well as to ensure proper operation of the comparator. Since, the control voltage (voltage equivalent to the control current scaled by the factor of sense resistance value) is supplied by the outer-voltage loop, the range of control voltage should be known for the control circuit design in the outer loop. The subject of control current for the inner-current loop of current-mode control scheme has not been well studied in the literature so far. The control-to-output transfer function of the inner loop is also required to design the outer loop as it is the plant transfer function for the outer loop.

In Chapter 2, the principle of peak current-mode operation is discussed. Using perturbation theory, the stability of the inner loop is analyzed. Considering the inner-current loop dynamics, sample-and-hold modeling is used to model the inner loop. The closed-loop control voltage-to-inductor current transfer function is derived in  $s$ -domain using modified Padé approximation. Chapter 3 presents a converter independent expression for loop gain of the inner-current loop. Chapters 4 and 5 present

the boundary between the stable and unstable operations, measure of relative stability, expressions for required slope compensation at a specified margin of stability, and expressions for control current for buck, boost, and buck-boost converters along with a design example for a peak current-mode controlled buck converter with inner-current loop only. The dynamic behavior of the peak current-mode controlled buck converter is presented in Chapter 6. The critical path power stage transfer functions, relevant inner-current loop transfer functions, and control-to-output transfer function of the buck converter are presented. Chapter 7 presents the summary and contributions of this research.

## 1.2 Objectives

The objectives of this research are:

1. To analyze the inner-current loop dynamics.
2. To derive a general expression for the loop gain of the inner-current loop, independent of the converter topology.
3. To determine the boundary between the stable and unstable regions of operation for the inner loop.
4. To derive an expression for the required slope compensation to achieve a specified margin of stability.
5. To derive expressions for control current for the inner loop of peak current-mode controlled dc-dc converters without and with slope compensation.
6. To analyze the dynamic behavior of the inner loop and to present relevant inner-current loop transfer functions.
7. To derive the control-to-output transfer function of the inner loop.

8. To validate the presented theories using Saber Sketch simulations and experimentation.

## 2 Peak Current-Mode Control

### 2.1 Principle of Operation

A peak current-mode controlled dc-dc converters consist of two loops: (a) an inner-current loop and (b) an outer-voltage loop. The inner-current loop directly controls the inductor current, which is a function of the load current for PWM dc-dc converters. Therefore, the inner-current loop indirectly controls the output voltage. The outer-voltage loop directly controls the output voltage and supplies the control voltage to the inner-current loop. A PWM dc-dc buck converter with peak current-mode control is shown in Fig. 2.1. The following analysis concentrates on the inner-current loop operation in peak current-mode controlled PWM dc-dc converters operating in continuous conduction mode (CCM).

The inner-current loop consists of a sense resistor  $R_s$ , a comparator, and a R-S flip-flop. The relevant waveforms to illustrate the principle of peak current-mode control is shown in Fig. 2.2. A clock signal  $v_{CLK}$  with a switching frequency  $f_s$  is supplied to the set terminal of the R-S flip-flop, which sets the flip-flop output  $v_Q$  high, turning the MOSFET ON. As the MOSFET conducts, the inductor current increases with a constant slope. The sensed inductor current  $R_s i_L$  is compared with a control voltage  $v_C = R_s i_C$  using the comparator, where  $i_L$  and  $i_C$  are the inductor current and the control current. The sensed inductor current is supplied to the non-inverting input and the control voltage is supplied to the inverting input of the comparator. When the sensed inductor current reaches the value of the control voltage, the output of the comparator goes high which in turn resets the R-S flip-flop output  $v_Q$  to low, which turns the MOSFET OFF. Now, the current in the inductor begin to decrease with a constant slope. Thus, the output pulse from the flip-flop sets the duty cycle  $d_T = D + d$  of the converter, where  $D$  is the steady-state duty cycle and  $d$  is the small-signal component.

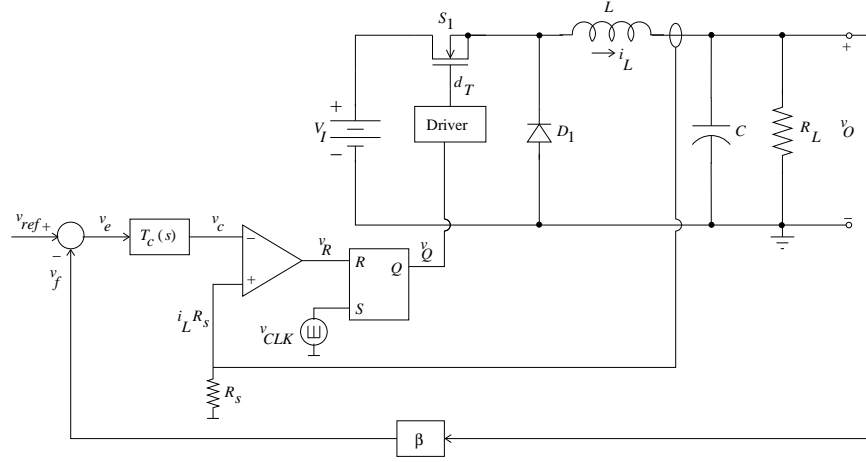


Figure 2.1: PWM dc-dc buck converter with peak current-mode control.

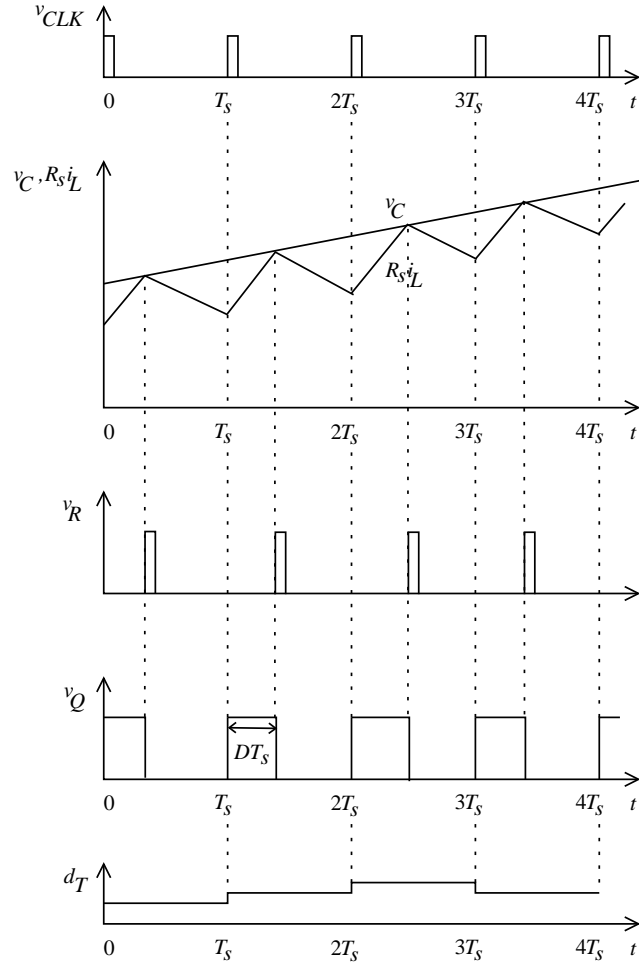


Figure 2.2: Relevant waveforms in the inner-current loop of peak current-mode controlled PWM dc-dc converter.

Thus, the turn-on of the MOSFET is decided by the clock signal which initiates the switching cycle at a constant frequency. The turn-off of the MOSFET is determined by the the level of control voltage and the intersection points of the peak value of sensed inductor current and the control voltage. Therefore, the duty ratio depends on the value of the control voltage as well as the time required by the peak value of the sensed inductor current to reach the control voltage. The inner-current loop consists of both analog (e.g.  $R_s i_L$ ,  $v_C$ ) and discrete (e.g.  $d_T$ ) signals. Therefore, current-mode controlled systems are true mixed-mode systems.

Depending on the required range of operating duty cycle, there are two different types of peak current-mode control available (a) without slope compensation and (b) with slope compensation. In the following sections, perturbation theory will be used for modeling and stability analysis of the peak-current mode controlled PWM dc-dc converters. It is assumed that the input and output voltages,  $V_I$  and  $V_O$ , of the converters remain constant. Thus, the inductor current on-slope  $M_1$  and off-slope  $M_2$ , which are dependent on the input and output voltages, remain constant.

## 2.2 Perturbation Ratio and Perturbation Coefficient

Fig. 2.3 shows the steady-state and perturbed inductor current waveforms in a peak current-mode controlled dc-dc converter. Let  $\Delta i_{L0}$  be the perturbation to the inductor current at  $t = 0$ .  $\Delta i_{L1}$  and  $\Delta i_{L2}$  are the resultant perturbations at the end of the first cycle and at the end of the second cycle, respectively.

Let  $a$  be the *perturbation ratio*, defined as the ratio of the perturbation at the end of the  $n$ th cycle to that at the beginning of the  $n$ th cycle, i.e.,

$$a = \frac{|\Delta i_{Ln}|}{|\Delta i_{L(n-1)}|}. \quad (2.1)$$

Let  $a_n$  be the *perturbation coefficient*, defined as the ratio of the perturbation at the

end of  $n$  cycle to that at the beginning of the first cycle, i.e.,

$$a_n = \frac{|\Delta i_{Ln}|}{|\Delta i_{L0}|} = \frac{\Delta i_{L1}}{\Delta i_{L0}} \frac{\Delta i_{L2}}{\Delta i_{L1}} \dots \frac{\Delta i_{Ln}}{\Delta i_{L(n-1)}} = a^n. \quad (2.2)$$

### 2.2.1 Stability Analysis

Using perturbation theory:

- For a stable system, the perturbed waveform converges to the steady-state waveform after  $n$  cycles. Therefore, for a stable inner-current loop,

$$\lim_{n \rightarrow \infty} a_n = \lim_{n \rightarrow \infty} \frac{|\Delta i_{Ln}|}{|\Delta i_{L0}|} = \lim_{n \rightarrow \infty} a^n = 0 \quad (2.3)$$

which results in

$$a < 1. \quad (2.4)$$

- For a marginally stable system, the perturbation at the end of  $n$  cycles remains the same as that at the beginning of the cycle. Therefore, for a marginally stable inner-current loop,

$$\lim_{n \rightarrow \infty} a_n = \lim_{n \rightarrow \infty} \frac{|\Delta i_{Ln}|}{|\Delta i_{L0}|} = \lim_{n \rightarrow \infty} a^n = 1 \quad (2.5)$$

which results in

$$a = 1. \quad (2.6)$$

- For an unstable system, the perturbed waveform diverges away from the steady-state waveform. Therefore, for an unstable inner-current loop,

$$\lim_{n \rightarrow \infty} a_n = \lim_{n \rightarrow \infty} \frac{|\Delta i_{Ln}|}{|\Delta i_{L0}|} = \lim_{n \rightarrow \infty} a^n > 1 \quad (2.7)$$

which results in

$$a > 1. \quad (2.8)$$



The steady-state and perturbed inductor current waveforms as well as the small-signal inductor current waveforms for stable, marginally stable, and unstable inner-current loop are shown in Figs. 2.3(a), (b), and (c), respectively. In the following sections, the perturbation factor will be used to develop the general theory for the stability of the inner-current loop of peak current-mode controlled PWM dc-dc converters.

### 2.2.2 Current-Mode Control Without Slope Compensation

Fig. 2.4 shows the control current and the inductor current waveforms at steady state and after a perturbation of  $\Delta i_{L0}$  to the inductor current at the beginning of the cycle for peak current-mode control without slope compensation.  $\Delta i_{L1}$  is the resultant perturbation at the end of the cycle. Let  $M_1$  and  $M_2$  be the on-slope and the off-slope of the inductor current, respectively. Also,  $D$  and  $T_s = \frac{1}{f_s}$  are the duty cycle and the period of operation for the converter, respectively.

Using the geometry in Fig. 2.4,

$$M_1 = \tan \alpha = \frac{\Delta i_L}{DT_s} = \frac{AC}{\Delta t_k}, \quad (2.9)$$

which gives

$$AC = \Delta i_{L0} = M_1 \Delta t_k = \frac{\Delta i_L}{DT_s} \Delta t_k. \quad (2.10)$$

Also,

$$M_2 = \tan \beta = \frac{\Delta i_L}{(1-D)T_s} = \frac{AB}{\Delta t_k}, \quad (2.11)$$

which gives

$$AB = \Delta i_{L1} = M_2 \Delta t_k = \frac{\Delta i_L}{(1-D)T_s} \Delta t_k. \quad (2.12)$$

Therefore, using (2.10) and (2.12), the perturbation ratio  $a$  is obtained as

$$a = \frac{\Delta i_{L1}}{\Delta i_{L0}} = \frac{AB}{AC} = \frac{M_2}{M_1} = \frac{D}{1-D}. \quad (2.13)$$

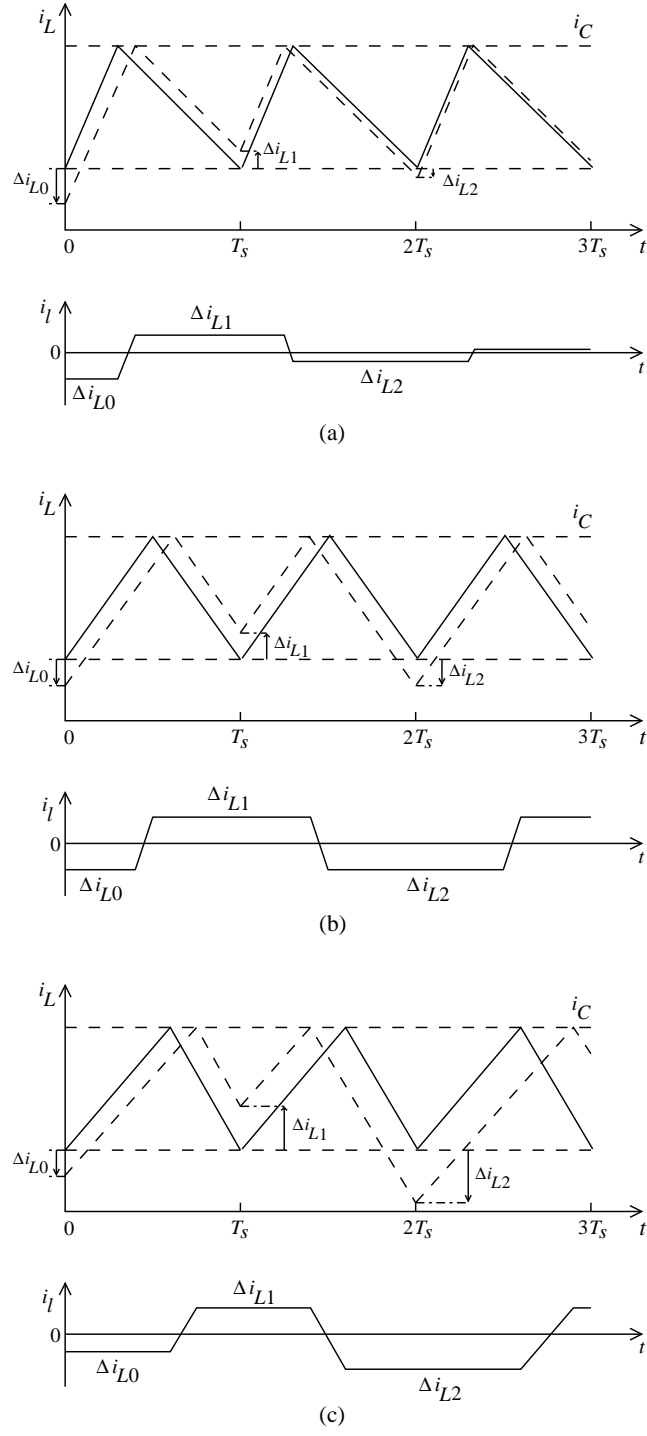


Figure 2.3: Steady-state (solid line) and perturbed (dashed line) inductor current waveforms. (a) Stable system,  $a < 1$ . (b) Marginally stable system,  $a = 1$ . (c) Unstable system,  $a > 1$ .

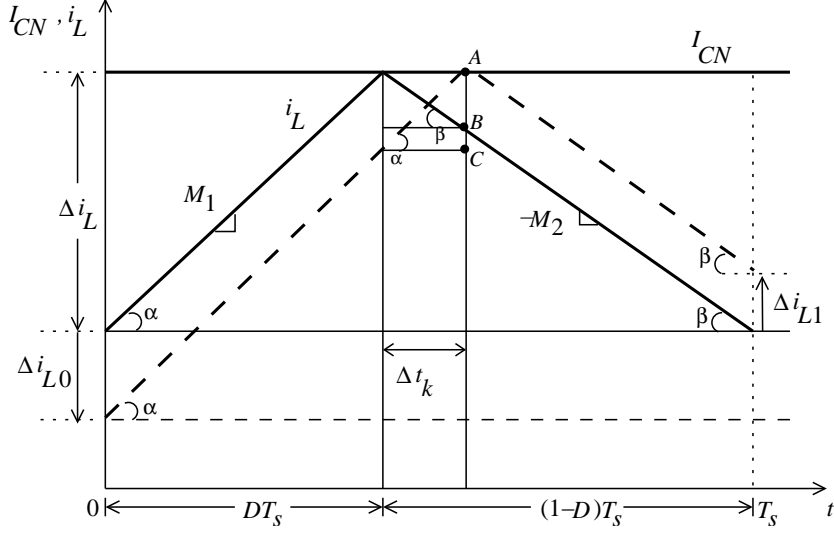


Figure 2.4: Steady-state (solid-line) and perturbed (dashed-line) waveforms of the inductor current for current-mode control without slope compensation.

Using (2.2) and (2.13), the perturbation coefficient  $a_n$  is

$$a_n = \frac{\Delta i_{Ln}}{\Delta i_{L0}} = a^n = \left( \frac{M_2}{M_1} \right)^n = \left( \frac{D}{1-D} \right)^n, \quad (2.14)$$

which is a geometric progression with a common ratio of  $\frac{D}{1-D}$ .

### 2.2.3 Current-Mode Control With Slope Compensation

The steady-state and perturbed waveforms of the inductor current as well as the control current waveform with a compensating ramp are shown in Fig. 2.5. Let  $M_1$ ,  $M_2$ , and  $M_3$  be the on-slope of the inductor current, the off-slope of the inductor current, and the compensation slope added to the control current, respectively. Also,  $\Delta i_{L0}$  and  $\Delta i_{L1}$  are the perturbations in the inductor current at the beginning and at the end of the cycle, respectively. As seen from the figure, by adding the compensation slope, the intersection point between the inductor current and the control current as well as the resultant value of duty cycle is changed. From Fig. 2.5,

$$M_1 = \tan \alpha = \frac{BD}{\Delta t_k}, \quad (2.15)$$

$$M_2 = \tan \beta = \frac{AC}{\Delta t_k}, \quad (2.16)$$

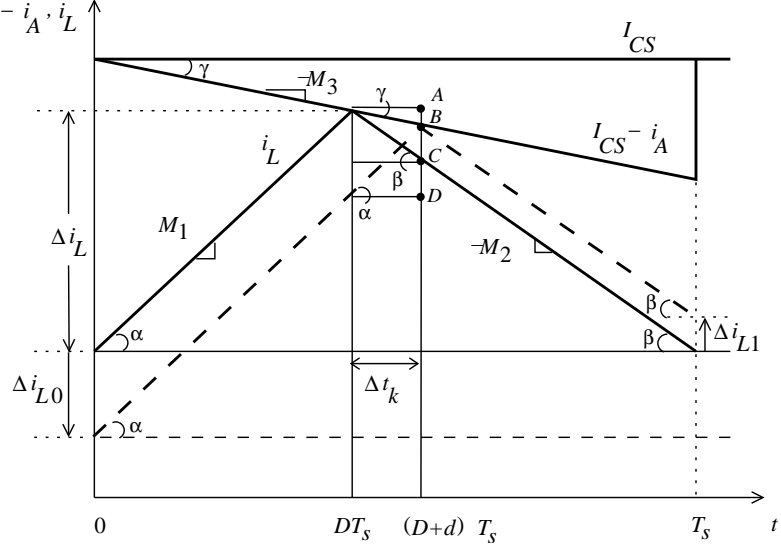


Figure 2.5: Steady-state (solid-line) and perturbed (dashed-line) waveforms of the inductor current for current-mode control with slope compensation.

and

$$M_3 = \tan \gamma = \frac{AB}{\Delta t_k}, \quad (2.17)$$

which gives

$$BD = M_1 \Delta t_k, \quad AC = M_2 \Delta t_k, \quad \text{and} \quad AB = M_3 \Delta t_k. \quad (2.18)$$

Also,

$$\Delta i_{L0} = AD = AB + BD = (M_1 + M_3) \Delta t_k \quad (2.19)$$

and

$$\Delta i_{L1} = BC = AC - AB = (M_2 - M_3) \Delta t_k. \quad (2.20)$$

Therefore, the perturbation ratio

$$\begin{aligned} a &= \frac{\Delta i_{L1}}{\Delta i_{L0}} = \frac{BC}{AD} = \frac{M_2 - M_3}{M_1 + M_3} \\ &= \frac{\frac{M_2}{M_1} - \frac{M_3}{M_1}}{1 + \frac{M_3}{M_1}} = \frac{\frac{D}{1-D} - \frac{M_3}{M_1}}{1 + \frac{M_3}{M_1}} \end{aligned} \quad (2.21)$$

is a function of duty cycle and slope compensation.

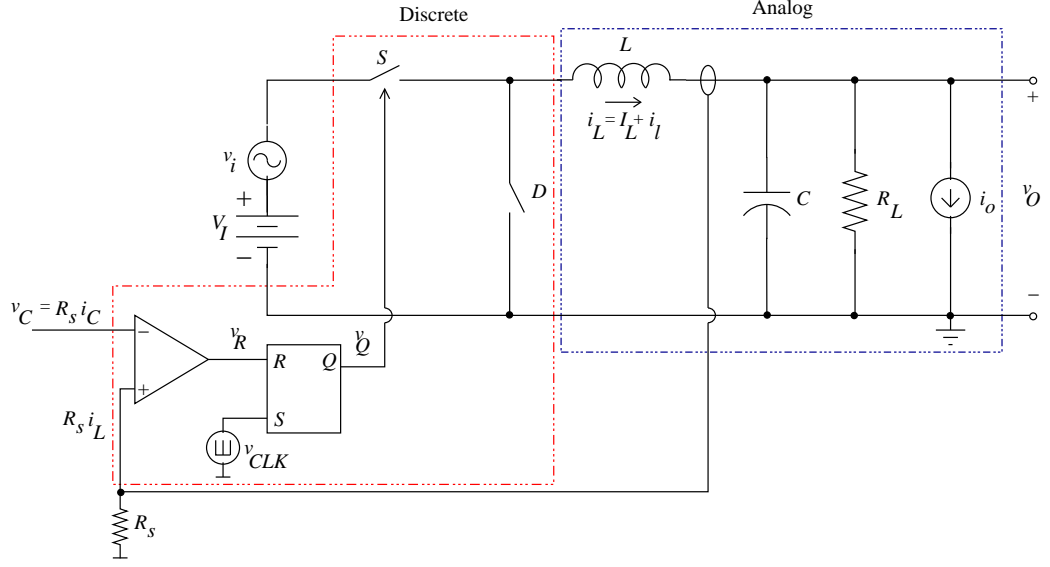


Figure 2.6: Peak current-mode controlled dc-dc buck converter with inner-current loop only.

### 2.3 Analysis of Inner-Current Loop Dynamics

A peak current-mode controlled PWM dc-dc buck converter with the inner-current loop only is shown in Fig. 2.6. The figure shows the analog and discrete components in the system. Therefore, the inner-current loop of the peak current-mode controlled dc-dc converters are true mixed-signal systems.

Fig. 2.7 shows steady-state (solid-line) and perturbed (dashed-line) waveforms of the inductor current  $i_L$ , control current  $i_C$  for current-mode control with slope compensation  $i_C - i_A$ , and exact ( $i_l$ ) and approximate ( $i_l^0$ ) waveforms of small-signal inductor current in CCM. Using the figure, the inner-current loop dynamics can be divided into three steps:

1. Sampling of control current  $i_C$  (or  $i_C - i_A$  in the case of slope compensation).
2. Transformation of the sampled small-signal control current value  $i_c$  into the small-signal inductor current value  $i_l$ .
3. Holding of the resulting value of  $i_l$  for a switching period, until the next sampling

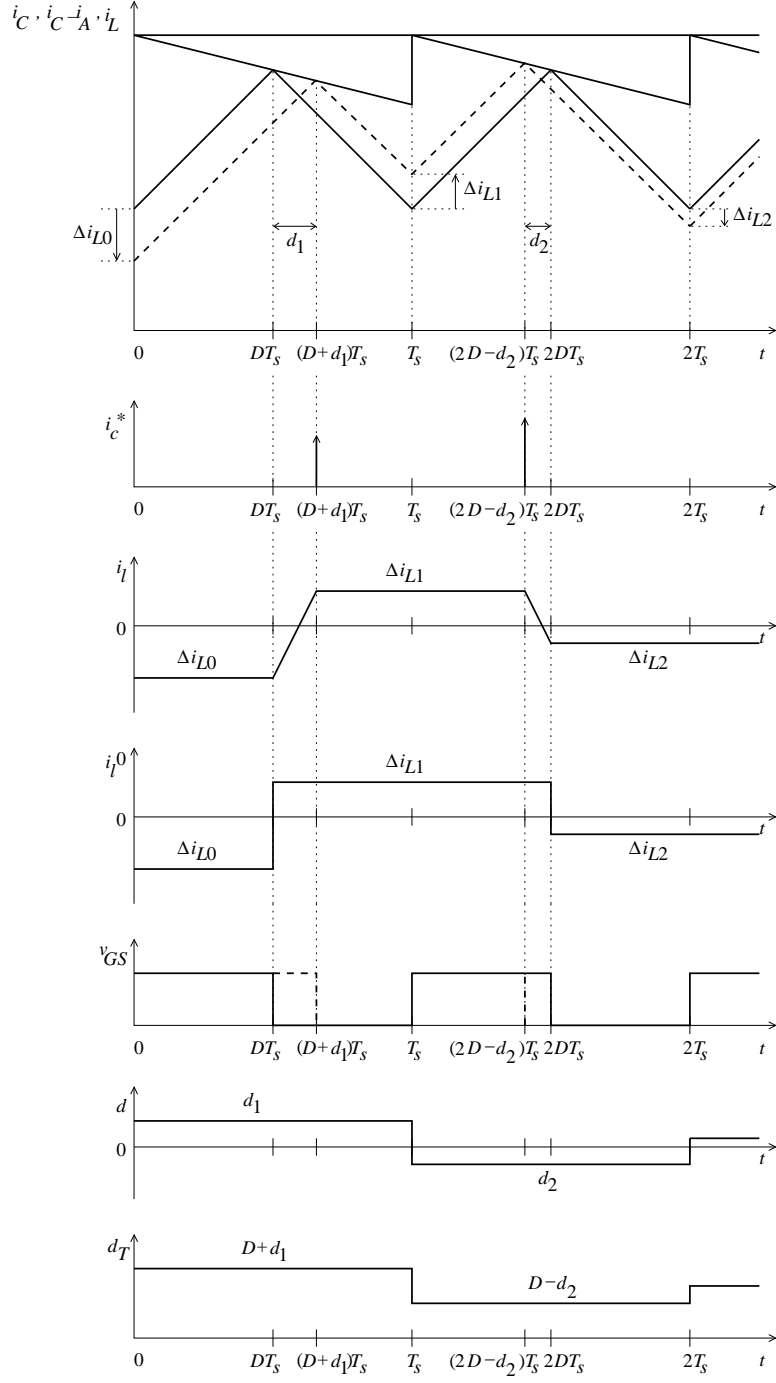


Figure 2.7: Steady-state (solid-line) and perturbed (dashed-line) waveforms of the inductor current  $i_L$ , control current  $i_C$  for current-mode control with slope compensation  $i_C - i_A$ , exact ( $i_l$ ) and approximate ( $i_l^0$ ) waveforms of small-signal inductor current, gate-to-source voltage  $v_{GS}$  waveform of the MOSFET, small-signal duty cycle  $d$  waveform and total duty cycle  $d_T$  waveform in CCM.

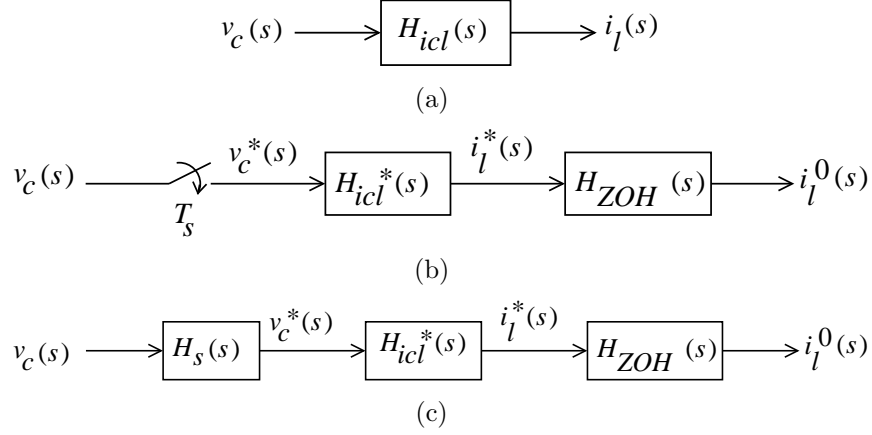


Figure 2.8: Block diagram of inner-current loop. (a) Closed loop transfer function. (b) Applying the inner-current loop dynamics. (c) Using sample and hold modeling.

instant.

Using the discrete nature of the system, the inner-current loop can be modeled in the z-domain.

## 2.4 Sample-and-Hold Modeling

Using the the inner-current loop dynamics and the discrete nature of the loop, the inner loop of the peak current-mode controlled dc-dc converters can be modeled using sample-and-hold modeling [7], [12], [19], [28]. Considering the control voltage as the input and inductor current as the output, the inner-current loop can be represented by a block diagram as shown in Fig. 2.8(a). The closed loop gain is defined as

$$H_{icl}(s) = \frac{i_l(s)}{v_c(s)}, \quad (2.22)$$

where  $i_l(s)$  is the small-signal inductor current and  $v_c(s) = R_s i_c(s)$  is the small-signal control voltage. Including the inner loop dynamics given in Section 2.3 and using equivalent-hold approximation [11], the block diagram in Fig. 8(a) can be expanded as shown in Fig. 8(b). The closed-loop gain is

$$H_{icl}(s) = \frac{i_l(s)}{v_c(s)} \approx \frac{v_c^*(s)}{v_c(s)} \times \frac{i_l^*(s)}{v_c^*(s)} \times \frac{i_l^0(s)}{i_l^*(s)} = H_s(s) \times H_{icl}^*(s) \times H_{ZOH}(s), \quad (2.23)$$

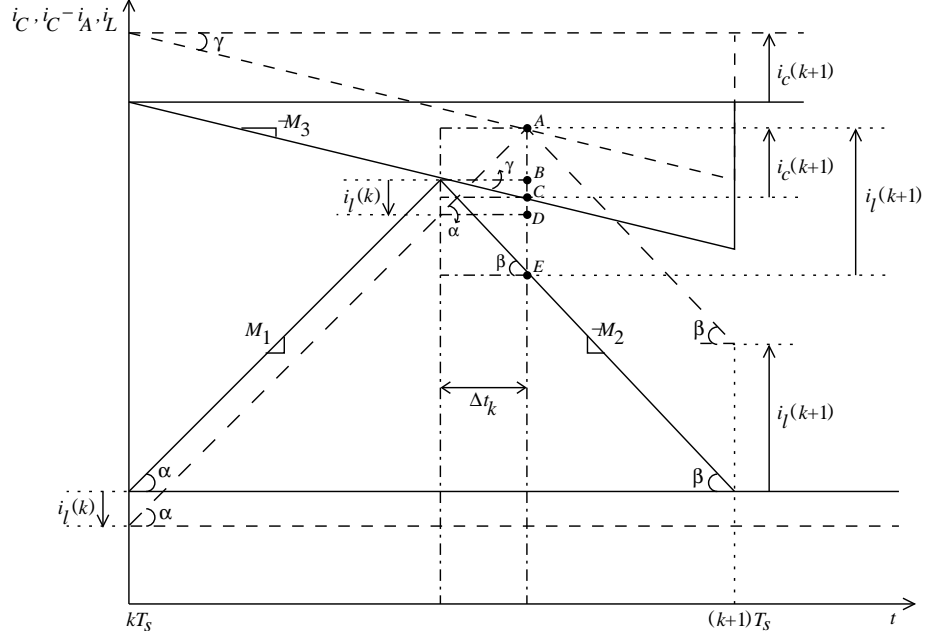


Figure 2.9: Steady state (solid line) and perturbed (dashed line) inductor current  $i_L$  and control current  $i_C, i_C - i_A$  waveforms.

where the sampling transfer function is

$$H_s(s) = \frac{v_c^*(s)}{v_c(s)} = \frac{1}{T_s}, \quad (2.24)$$

the discrete closed-loop control voltage-to-inductor current transfer function is

$$H_{icl}^*(s) = H_{icl}(z) \Big|_{z=e^{sT_s}} = \frac{i_L^*(s)}{v_c^*(s)}, \quad (2.25)$$

and the zero-order hold transfer function is

$$H_{ZOH}(s) = \frac{i_L^0(s)}{i_L^*(s)} \approx \frac{i_L(s)}{i_L^*(s)} = \frac{1 - e^{-sT_s}}{s}. \quad (2.26)$$

Since, the sampling and zero-order hold transfer functions are known, the only unknown transfer function to obtain the closed-loop gain  $H_{icl}(s)$  is the discrete closed-loop gain  $H_{icl}^*(s) = H_{icl}(z) \Big|_{z=e^{sT_s}}$ .

## 2.5 Discrete Closed-Loop Transfer Function $H_{icl}(z)$

Steady state (solid line) and perturbed (dashed line) inductor current  $i_L$  and control current  $i_C, i_C - i_A$  waveforms in a peak current-mode controlled system is shown in



Fig. 2.9. Using the geometry,

$$M_1 = \tan \alpha = \frac{AD}{\Delta t_k}, \quad (2.27)$$

$$M_2 = \tan \beta = \frac{BE}{\Delta t_k}, \quad (2.28)$$

and

$$M_3 = \tan \gamma = \frac{BC}{\Delta t_k}, \quad (2.29)$$

which gives

$$AD = M_1 \Delta t_k, \quad BE = M_2 \Delta t_k, \quad \text{and} \quad BC = M_3 \Delta t_k, \quad (2.30)$$

respectively. Also,

$$BD = -i_l(k), \quad AE = i_l(k+1), \quad \text{and} \quad AC = i_c(k+1). \quad (2.31)$$

Also, from Fig. 2.9,

$$AB = AD - BD = M_1 \Delta t_k - [-i_l(k)] = M_1 \Delta t_k + i_l(k), \quad (2.32)$$

$$AB = AE - BE = i_l(k+1) - M_2 \Delta t_k, \quad (2.33)$$

and

$$AB = AC - BC = i_c(k+1) - M_3 \Delta t_k. \quad (2.34)$$

Subtracting (2.32) from (2.34) gives

$$i_c(k+1) - M_3 \Delta t_k - M_1 \Delta t_k - i_l(k) = 0 \quad (2.35)$$

which leads to

$$(M_1 + M_3) \Delta t_k = i_c(k+1) - i_l(k). \quad (2.36)$$

Using (2.27)-(2.34),

$$\begin{aligned} i_l(k+1) &= AE = AD + DE = AD + (BE - BD) \\ &= M_1 \Delta t_k + M_2 \Delta t_k - [-i_l(k)] \end{aligned}$$

$$\begin{aligned}
&= M_1 \Delta t_k + M_3 \Delta t_k + M_2 \Delta t_k - M_3 \Delta t_k + i_l(k) \\
&= (M_1 + M_3) \Delta t_k + (M_2 - M_3) \Delta t_k + i_l(k) \\
&= (M_1 + M_3) \Delta t_k + \frac{M_2 - M_3}{M_1 + M_3} (M_1 + M_3) \Delta t_k + i_l(k). \tag{2.37}
\end{aligned}$$

Substituting (2.21) and (2.36) into (2.37),

$$\begin{aligned}
i_l(k+1) &= (M_1 + M_3) \Delta t_k + a(M_1 + M_3) \Delta t_k + i_l(k) \\
&= (1+a)(M_1 + M_3) \Delta t_k + i_l(k) \\
&= (1+a)[i_c(k+1) - i_l(k)] + i_l(k) \\
&= (1+a)i_c(k+1) - ai_l(k). \tag{2.38}
\end{aligned}$$

Therefore,

$$i_l(k+1) = -ai_l(k) + (1+a)i_c(k+1). \tag{2.39}$$

But  $i_c(k+1) = \frac{v_c(k+1)}{R_s}$ . Thus,

$$i_l(k+1) = -ai_l(k) + \frac{1+a}{R_s} v_c(k+1). \tag{2.40}$$

Taking  $z$ -transform on both sides of (2.40) gives

$$zi_l(z) = -ai_l(z) + \frac{1+a}{R_s} zv_c(z), \tag{2.41}$$

which results in

$$(z+a)i_l(z) = \frac{1+a}{R_s} zv_c(z). \tag{2.42}$$

Therefore, the discrete closed-loop transfer function in  $z$ -domain is obtained as

$$H_{icl}(z) = \frac{i_l(z)}{v_c(z)} = \frac{1+a}{R_s} \frac{z}{z+a}. \tag{2.43}$$

Thus, the inner-current loop is a closed-loop system with a zero at the origin and a pole at  $z = -a$ .

The stability of a system in  $z$ -domain is analyzed by the position of the closed-loop pole in the unit circle. The system is stable when the pole lies inside the circle, is

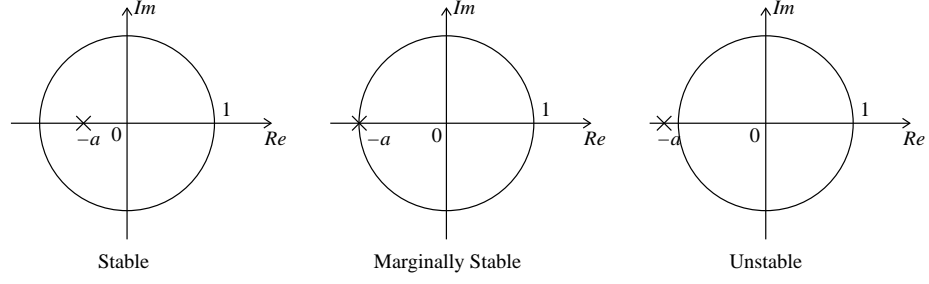


Figure 2.10: Position of the z-domain closed-loop pole  $a$  in the unit circle for stable, marginally stable, and unstable inner loop.

marginally stable when the pole lies on the circle, and is unstable when the pole lies outside the unit circle. Therefore, the inner-loop is stable for  $a < 1$ , is marginally stable for  $a = 1$ , and is unstable for  $a > 1$ , which agrees with the analysis in Section 2.2.1. Fig. 2.10 shows the position the closed-loop pole  $a$  in the unit circle for stable, marginally stable, and unstable inner-current loop.

## 2.6 Closed-Loop Control Voltage-to-Inductor Current Transfer Function $H_{icl}(s)$

Substituting  $z = e^{sT_s}$  into (2.43) gives

$$H_{icl}^*(s) = H_{icl}(z) \Big|_{z=e^{sT_s}} = \frac{i_l^*(s)}{v_c^*(s)} = \frac{1+a}{R_s} \frac{e^{sT_s}}{e^{sT_s} + a}. \quad (2.44)$$

Substituting (2.24)-(2.26) and (2.44) into (2.23), we obtain [11], [12], [19], [28], [34]

$$\begin{aligned} H_{icl}(s) &= H_s(s) \times H_{icl}^*(s) \times H_{ZOH}(s) \\ &= \frac{1+a}{R_s T_s} \frac{e^{sT_s} - 1}{s(e^{sT_s} + a)}. \end{aligned} \quad (2.45)$$

The closed-loop transfer function  $H_{icl}(s)$  obtained in (2.45) is in exponential form. The obtained transfer function is non-rational. To convert (2.45) into a rational form, approximations available for  $e^{-sT_s}$  are considered. A Taylor series approximation of  $e^{-sT_s}$  in (2.45) results in just zeroes and no poles, resulting in an improper transfer function. To avoid this situation, a polynomial approximation for  $e^{-sT_s}$ , Padé

approximation is considered. The first-order Padé approximation is given by

$$e^{-sT_s} = \frac{1 - \frac{sT_s}{2}}{1 + \frac{sT_s}{2}}, \quad (2.46)$$

the second-order Padé approximation is given by

$$e^{-sT_s} = \frac{1 - \frac{sT_s}{2} + \frac{(sT_s)^2}{12}}{1 + \frac{sT_s}{2} + \frac{(sT_s)^2}{12}}, \quad (2.47)$$

and the third-order Padé approximation is given by

$$e^{-sT_s} = \frac{1 - \frac{sT_s}{2} + \frac{(sT_s)^2}{10} - \frac{(sT_s)^3}{120}}{1 + \frac{sT_s}{2} + \frac{(sT_s)^2}{10} + \frac{(sT_s)^3}{120}}. \quad (2.48)$$

A second-order modified Padé approximation which is given by

$$e^{-sT_s} = \frac{1 - \frac{sT_s}{2} + \frac{(sT_s)^2}{\pi^2}}{1 + \frac{sT_s}{2} + \frac{(sT_s)^2}{\pi^2}}. \quad (2.49)$$

### 2.6.1 Comparison of the Actual Function $e^{sT_s}$ and the Approximations

A comparison of the actual function  $e^{sT_s}$  and different orders of Padé approximations in a semilog scale obtained using MatLab simulations is illustrated in Fig. 2.11(a). In Fig. 2.11(b), the comparison is shown in a linear scale. As seen from the plots, the first order Padé approximation follows the actual function till  $0.1f_s$ , which is not sufficient. The second order Padé approximation agrees with the actual function till half the switching frequency. On the other hand, the third order approximation holds well till  $f \approx f_s$ . Usage of higher order approximations is not difficult in analysis using Matlab. However, considering the simplicity in calculations as well as the accuracy till half the switching frequency, the second order Padé approximation is chosen for the further analysis.

A comparison of the actual function  $e^{sT_s}$  and the second order approximations

1. Padé approximation:

$$e^{sT_s} = \frac{1 + \frac{sT_s}{2} + \frac{(sT_s)^2}{12}}{1 - \frac{sT_s}{2} + \frac{(sT_s)^2}{12}} \quad (2.50)$$

and

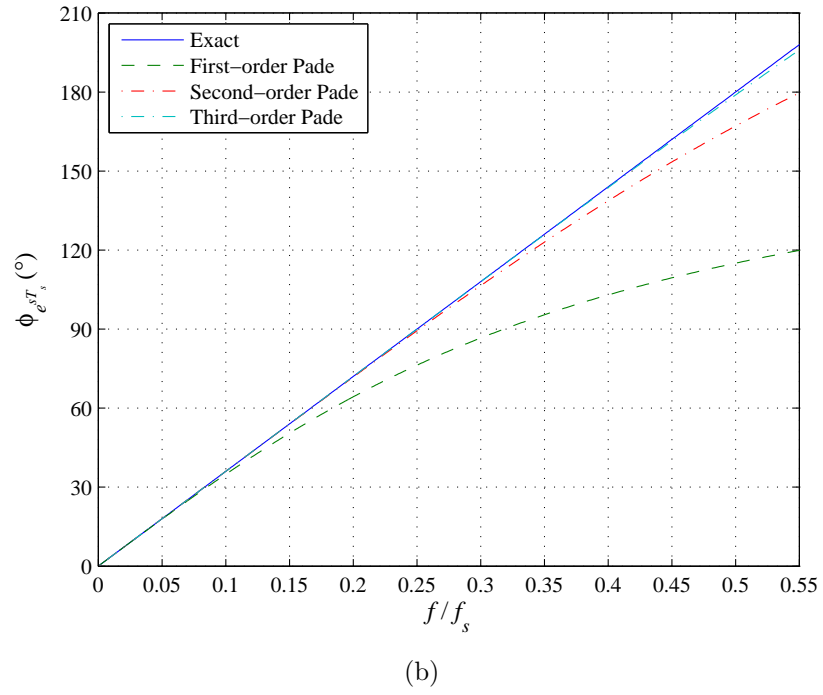
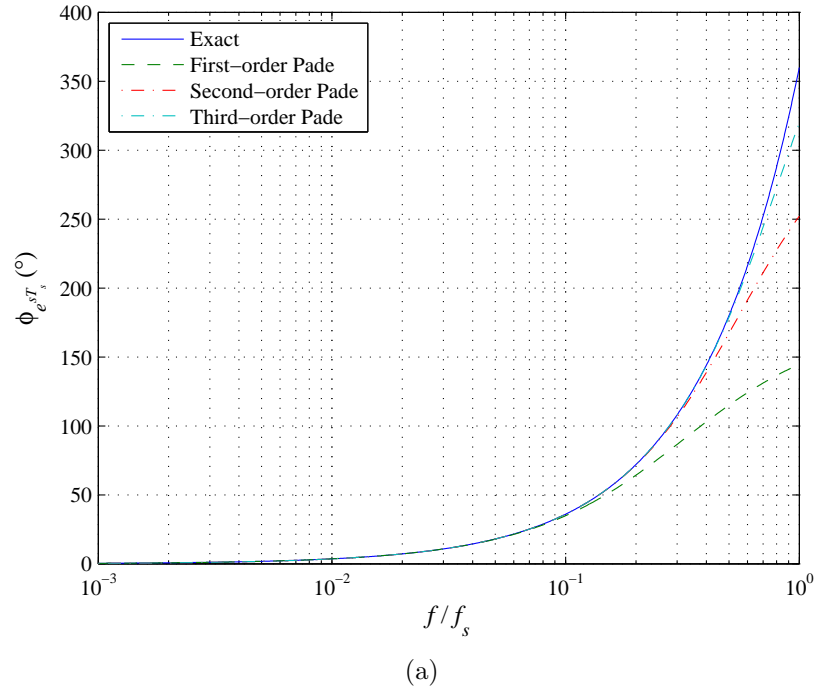
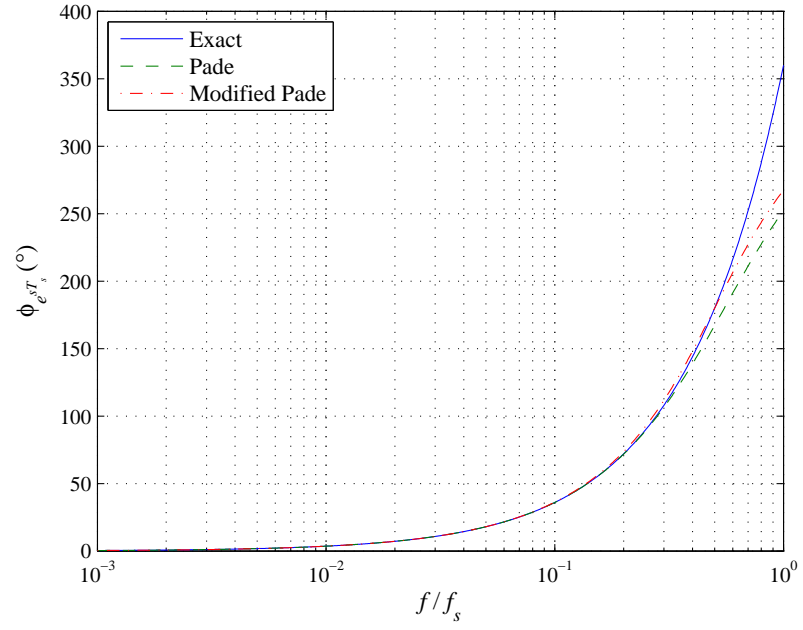
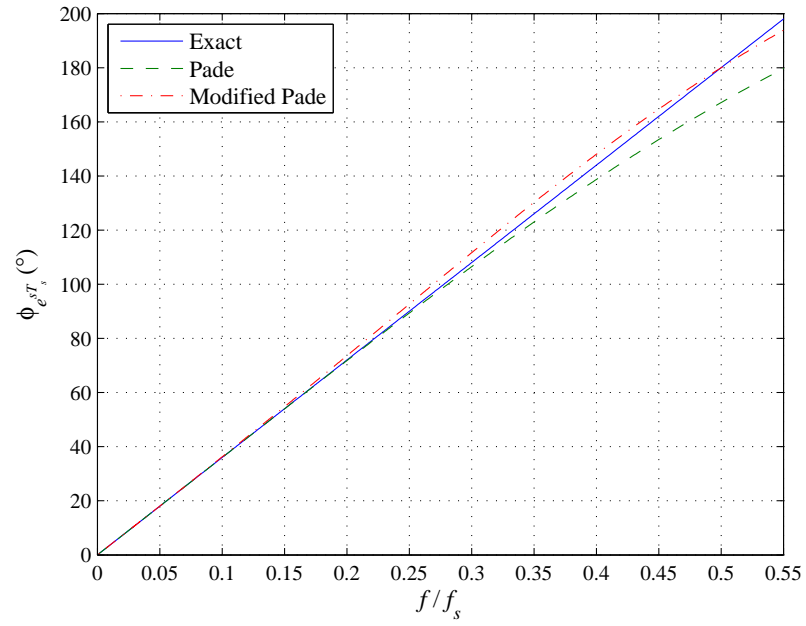


Figure 2.11: Comparison of the actual function  $e^{sT_s}$ , the first, second and third-order Padé approximations. (a) Semilog scale. (b) Linear scale.



(a)



(b)

Figure 2.12: Comparison of the actual function  $e^{sT_s}$ , the second order Padé approximation, and the second order modified Padé approximations. (a) Semilog scale. (b) Linear scale.

2. Modified Padé approximation:

$$e^{sT_s} = \frac{1 + \frac{sT_s}{2} + \frac{(sT_s)^2}{\pi^2}}{1 - \frac{sT_s}{2} + \frac{(sT_s)^2}{\pi^2}} \quad (2.51)$$

in a semilog scale is illustrated in Fig. 2.12(a). In Fig. 2.12(b), the comparison is shown in a linear scale. In both the figures, it is seen that while both the approximations follow the actual function till  $f_s/2$ , the modified Padé approximation has the same value as the actual function at  $f_s/2$ , as seen in Fig. 2.12(b). Also, as observed in both the figures, the modified Padé approximation provides an over-estimation and the Padé approximation provides an under-estimation of the actual function till  $f_s/2$ . In the higher frequencies, the approximations diverge away from the actual function.

### 2.6.2 Comparison of the Actual Function $H_{icl}(s)$ and the Approximations

The Bode plots of the exact function and the approximations of  $H_{icl}(s)$  are shown in Fig. 2.13. As seen in the figure, for frequencies lower than half the switching frequency, the approximations and the exact function are equal. From the enlarged plots shown in Fig. 2.14, the approximations agree with the exact expression very well till  $f = f_s/2$ . It is seen from the plots that the magnitude of the actual closed-loop transfer function is 0 dB at low frequencies and at integer multiples of the switching frequencies  $nf_s$ , it goes to negative infinity. From the phase plots it is noticed that at every integer multiples of the switching frequency  $nf_s$ , for the actual function an additional  $180^\circ$  is added to the phase. Fig. 2.15 shows the magnitude and phase plots of the closed loop transfer function in a linear scale. The magnitude and phase plots of the actual function resemble the magnitude and phase plots of the sample and hold transfer function. Also, it shows that the approximations are valid till half the switching frequency, the Nyquist frequency, which agrees with the sampling theorem.

For the following analysis, the modified Padé approximation will be employed to model the inner-current loop of the current-mode controlled PWM dc-dc converters.

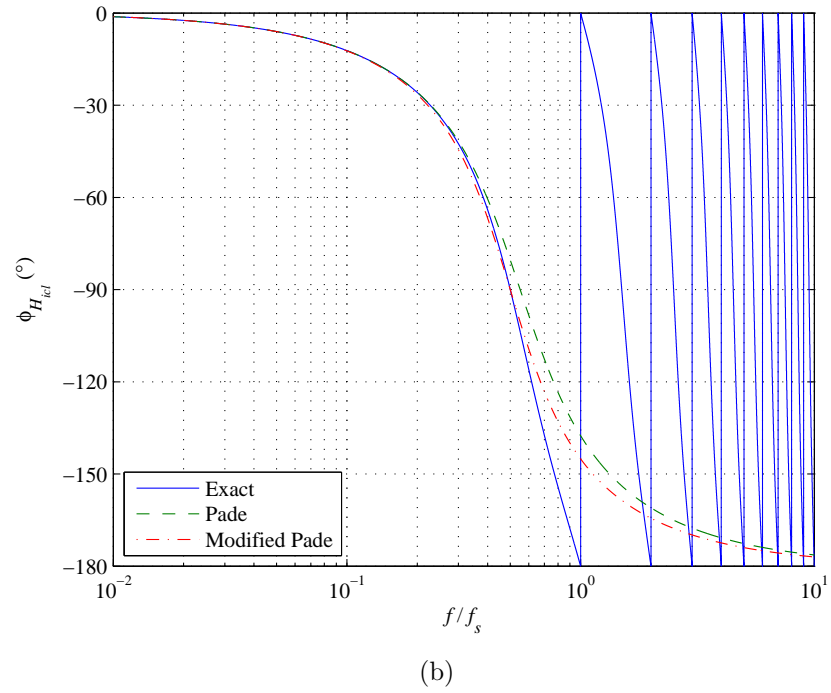
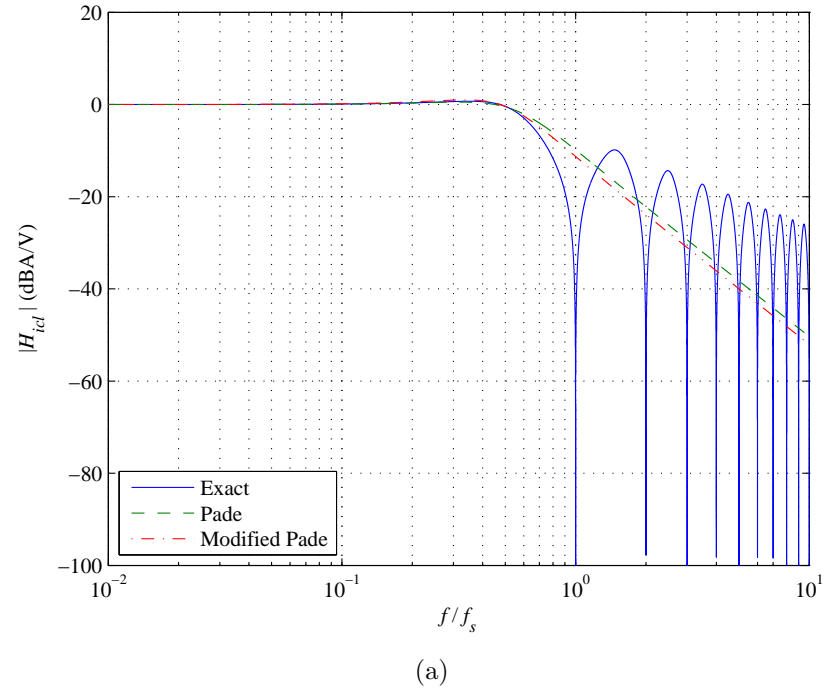
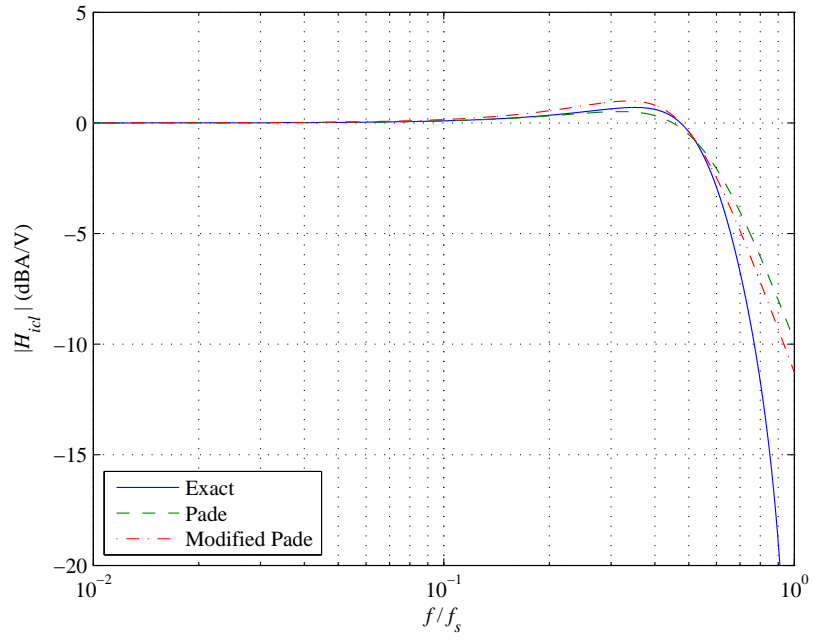
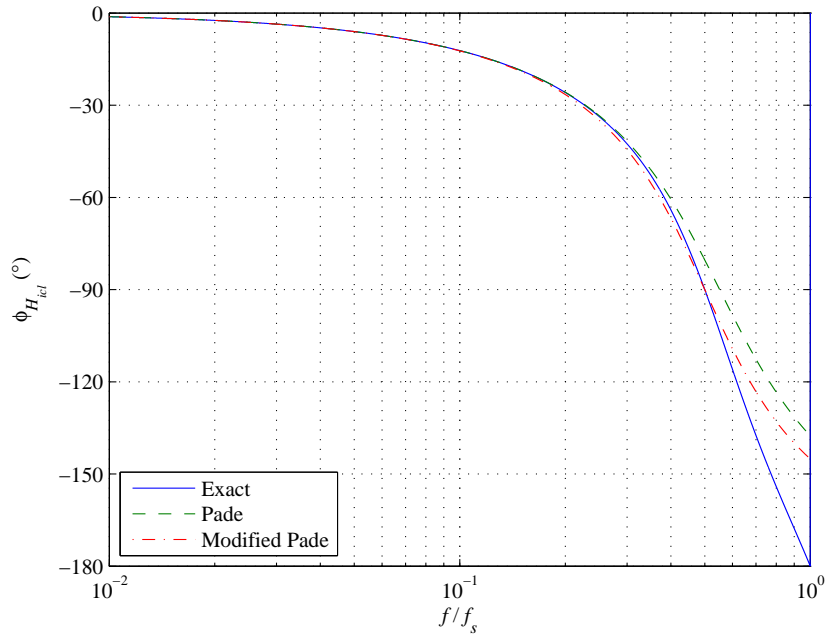


Figure 2.13: Comparison of Bode plots of the actual function  $H_{icl}(s)$ , the second-order Padé approximation, and the second-order modified Padé approximation at  $a = 0.2$ . (a) Magnitude. (b) Phase.





(a)



(b)

Figure 2.14: Comparison of enlarged Bode plots of the actual function  $H_{icl}(s)$ , the second-order Padé approximation, and the second-order modified Padé approximation at  $a = 0.2$ . (a) Magnitude. (b) Phase.

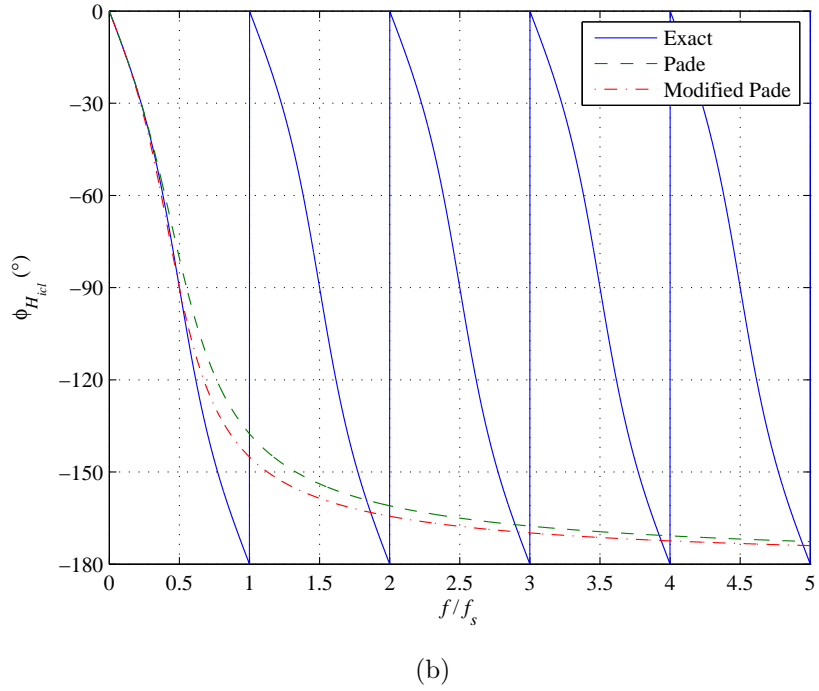
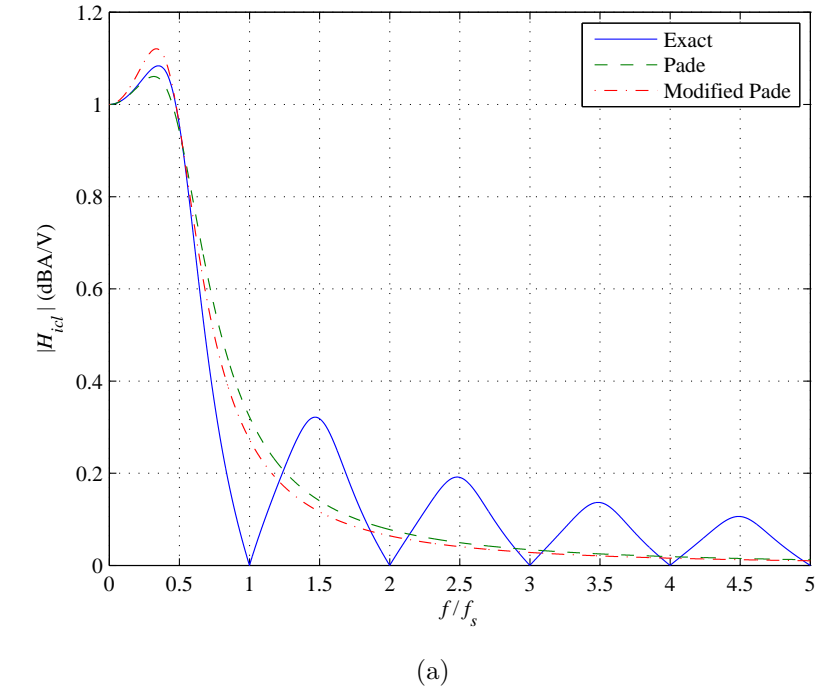


Figure 2.15: Comparison of the actual function  $H_{icl}(s)$ , the second-order Padé approximation, and the second-order modified Padé approximation in a linear scale at  $a = 0.2$ . (a) Magnitude. (b) Phase.

### 2.6.3 Closed Inner-Current Loop Transfer Function $H_{icl}(s)$

Substituting (2.51) into (2.45), the closed inner-current loop transfer function in the pole-zero format is obtained as

$$\begin{aligned}
 H_{icl}(s) &= \frac{i_l(s)}{v_c(s)} = \frac{1+a}{sR_sT_s} \frac{e^{sT_s} - 1}{e^{sT_s} + a} \\
 &= \left( \frac{1+a}{sR_sT_s} \right) \frac{\frac{1+\frac{sT_s}{2}+\frac{(sT_s)^2}{\pi^2}}{1-\frac{sT_s}{2}+\frac{(sT_s)^2}{\pi^2}} - 1}{\frac{1+\frac{sT_s}{2}+\frac{(sT_s)^2}{\pi^2}}{1-\frac{sT_s}{2}+\frac{(sT_s)^2}{\pi^2}} + a} \\
 &= \left( \frac{1+a}{sR_sT_s} \right) \frac{1+\frac{sT_s}{2}+\frac{(sT_s)^2}{\pi^2} - \left(1-\frac{sT_s}{2}+\frac{(sT_s)^2}{\pi^2}\right)}{1+\frac{sT_s}{2}+\frac{(sT_s)^2}{\pi^2} + a\left(1-\frac{sT_s}{2}+\frac{(sT_s)^2}{\pi^2}\right)} \\
 &= \left( \frac{1+a}{sR_sT_s} \right) \frac{sT_s}{(1+a) + (1-a)\frac{sT_s}{2} + (1+a)\frac{(sT_s)^2}{\pi^2}} \\
 &= \frac{1}{R_s} \frac{1}{1 + \frac{1-a}{1+a} \frac{s}{2f_s} + \frac{s^2}{\pi^2 f_s^2}} \\
 &= \frac{1}{R_s} \frac{\pi^2 f_s^2}{s^2 + \frac{\pi^2}{2} \frac{1-a}{1+a} f_s s + \pi^2 f_s^2}. \tag{2.52}
 \end{aligned}$$

Thus, the closed inner-current loop transfer function in the pole-zero format is derived as

$$H_{icl}(s) = \frac{1}{R_s} \frac{\omega_h^2}{s^2 + 2\xi_h\omega_h s + \omega_h^2}, \tag{2.53}$$

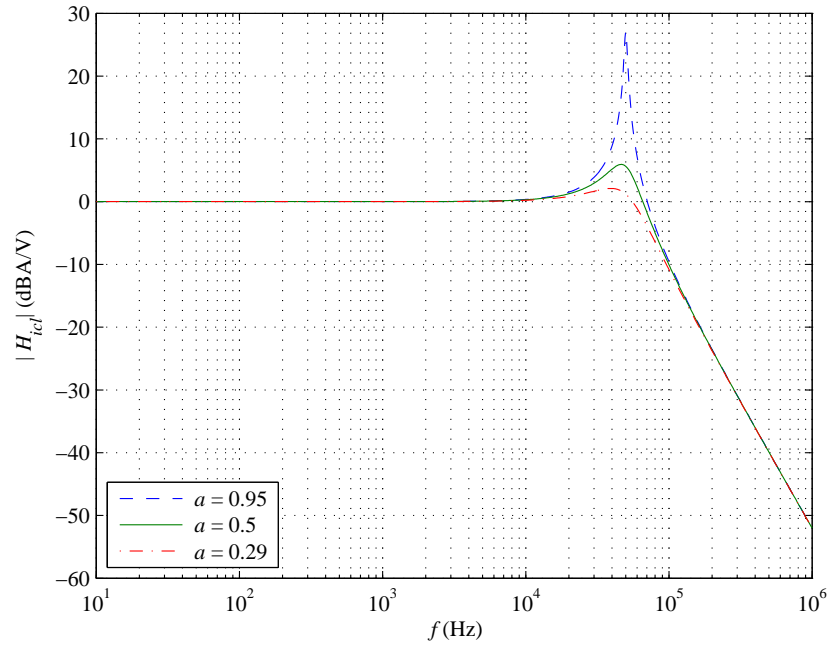
where the angular corner frequency and damping coefficient, respectively, are

$$\omega_h = \pi f_s \text{ and } \xi_h = \frac{\pi}{4} \frac{1-a}{1+a}. \tag{2.54}$$

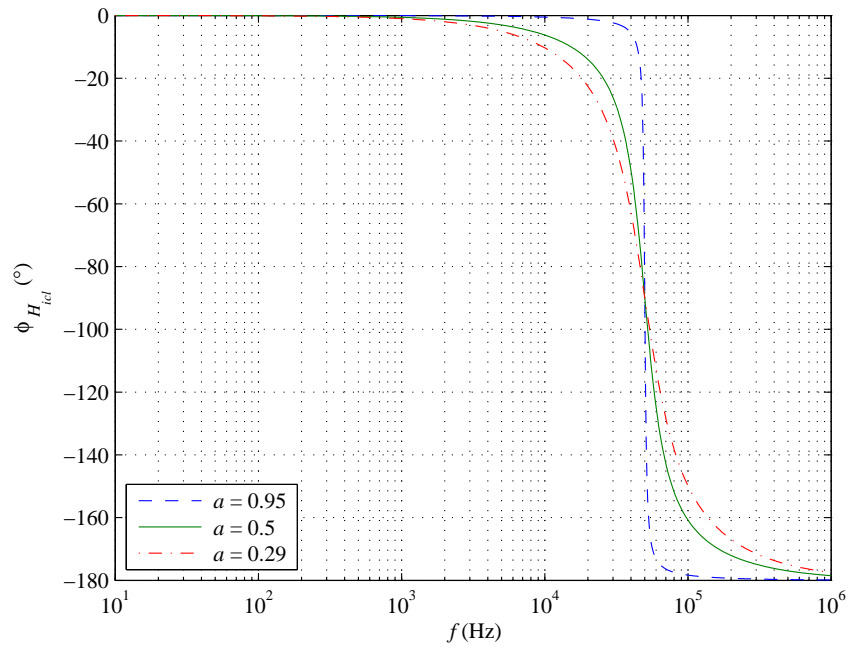
Fig. 2.16 shows the Bode plots of the closed-loop transfer function  $H_{icl}(s)$  at  $a = 0.29$ ,  $a = 0.5$ , and  $a = 0.95$ .

### 2.6.4 Experimental Results

A buck converter with inner-current loop without slope compensation was set up. The design had the following parameters:  $V_O = 7$  V,  $I_O = 0.7$  A,  $L = 258$   $\mu$ H,



(a)



(b)

Figure 2.16: Bode plots of the closed-loop gain  $H_{icl}(s)$  at  $a = 0.29$ ,  $a = 0.5$ , and  $a = 0.95$ . (a) Magnitude. (b) Phase.

Table 2.1:  $V_I$ ,  $D$ ,  $V_C$ , and  $a$  used in the experimental measurement.

$V_I$	$D$	$V_C$	$a = \frac{D}{1-D}$
16	0.487	0.777	0.95
23	0.333	0.797	0.5
35	0.23	0.81	0.299

$r_L = 36 \text{ m}\Omega$ ,  $C = 68 \text{ }\mu\text{F}$ ,  $r_C = 520 \text{ m}\Omega$ ,  $R_L = 10 \text{ }\Omega$ ,  $r_{DS} = 0.4 \text{ }\Omega$ ,  $R_F = 0.1 \text{ }\Omega$ ,  $V_F = 0.7 \text{ }\Omega$ ,  $R_s = 1 \text{ }\Omega$  and  $f_s = 100 \text{ kHz}$ . The MOSFET delay was measured as  $t_d = 1 \text{ }\mu\text{s}$ . Table 2.1 shows the values of  $a$  corresponding to the selected values of  $V_I$  and  $D$ .

The Bode plots of control voltage-to-inductor current transfer function were measured using Hewlett-Packard 4194A Impedance/Gain-Phase Analyzer and Pearson model 411 wide-bandwidth current probe. The probe frequency response was measured using a simple resistive load of  $R_L = 1 \text{ }\Omega$  and the same dc current as in the buck converter design  $I = 0.7 \text{ A}$ . The effect of the probe frequency response on the measured  $H_{icl}$  response was compensated using the compensation function of the 4194A analyzer. Fig. 2.17(a), (b), and (c) shows the resultant Bode plots for  $a = 0.29$ ,  $a = 0.5$ , and  $a = 0.95$ , respectively. The experimental Bode plots show excellent agreement with the theoretical Bode plots shown in Fig. 2.16.

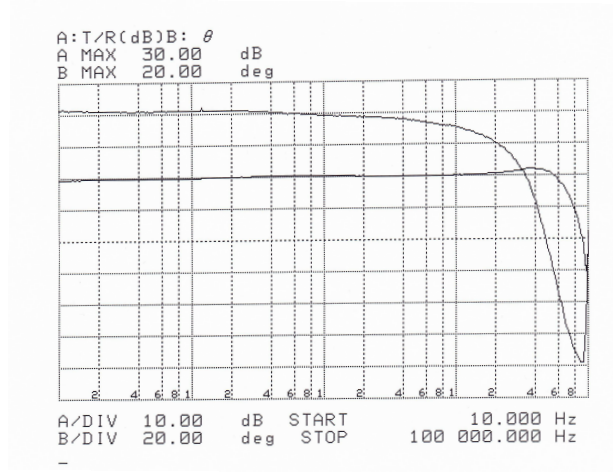
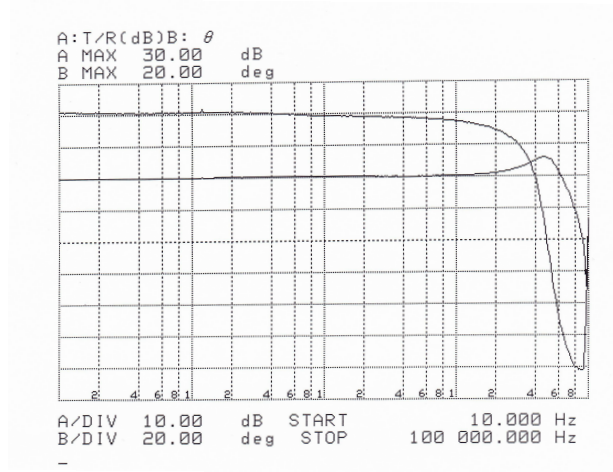
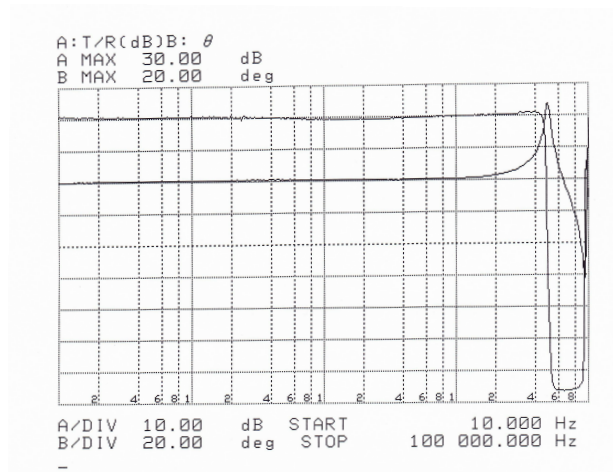
(a)  $a = 0.29$ (b)  $a = 0.5$ (c)  $a = 0.95$ 

Figure 2.17: Experimental Bode plots of the closed-loop gain  $H_{icl}(s)$  at  $a = 0.29$ ,  $a = 0.5$ , and  $a = 0.95$ .

### 3 Loop Gain of Inner-Current Loop

#### 3.1 Structure of the Inner-Current Loop

A closed-loop structure with feedback is assumed for the inner-current loop to analyze the margins of stability of the loop. The assumed structure for the inner-current loop of peak current-mode controlled PWM dc-dc converters is shown in Fig. 3.1, where  $v_c(s)$  is the small-signal control voltage,  $v_e(s)$  is the error voltage,  $i_l(s)$  is the small-signal inductor current,  $H_{icl}(s) = \frac{i_l(s)}{v_c(s)}$  is the closed-loop gain,  $T_f(s) = \frac{i_l(s)}{v_e(s)}$  is the forward-path gain,  $T_i(s) = \frac{R_s i_l(s)}{v_e(s)}$  is the loop gain, and  $R_s$  is the sense resistor.

Using block reduction in basic control theory in Fig. 3.1, the closed-loop gain is

$$H_{icl}(s) = \frac{i_l(s)}{v_c(s)} = \frac{T_f(s)}{1 + T_f(s)R_s} = \frac{\frac{T_i(s)}{R_s}}{1 + T_i(s)}. \quad (3.1)$$

Therefore, we obtain the forward-path gain

$$T_f(s) = \frac{i_l(s)}{v_e(s)} = \frac{H_{icl}(s)}{1 - H_{icl}(s)R_s} \quad (3.2)$$

and the loop gain

$$T_i(s) = \frac{R_s i_l(s)}{v_e(s)} = T_f(s)R_s = \frac{H_{icl}(s)R_s}{1 - H_{icl}(s)R_s}. \quad (3.3)$$

#### 3.2 General Expression for Loop Gain of Inner-Current Loop

An expression for the loop gain of the inner-current loop is necessary to analyze the stability margins of the inner loop. Substituting (2.45) into (3.3), the expression for

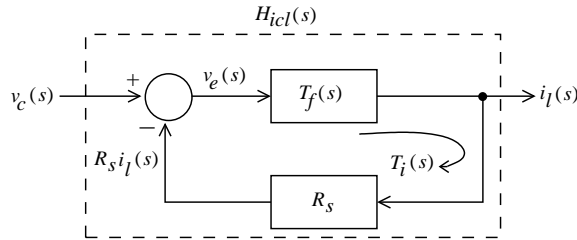
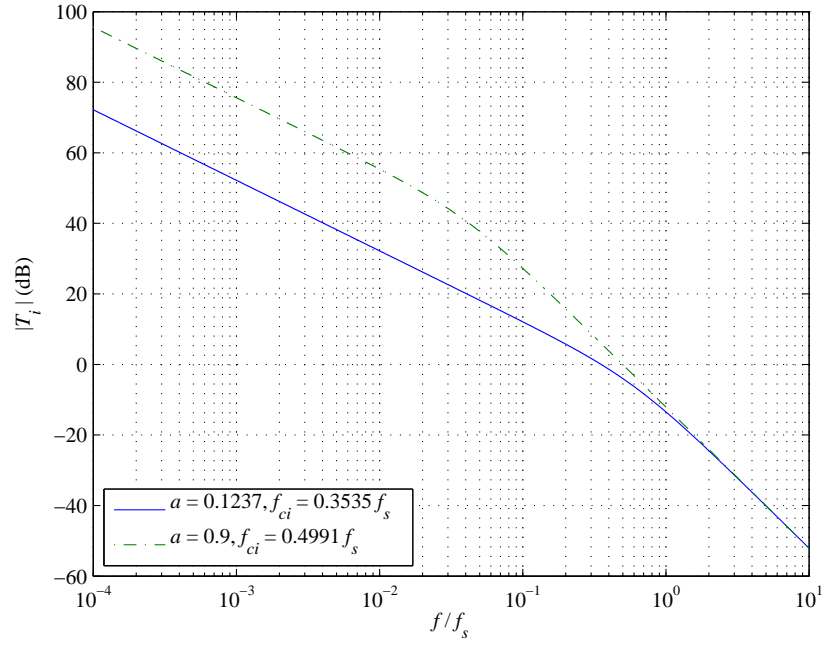
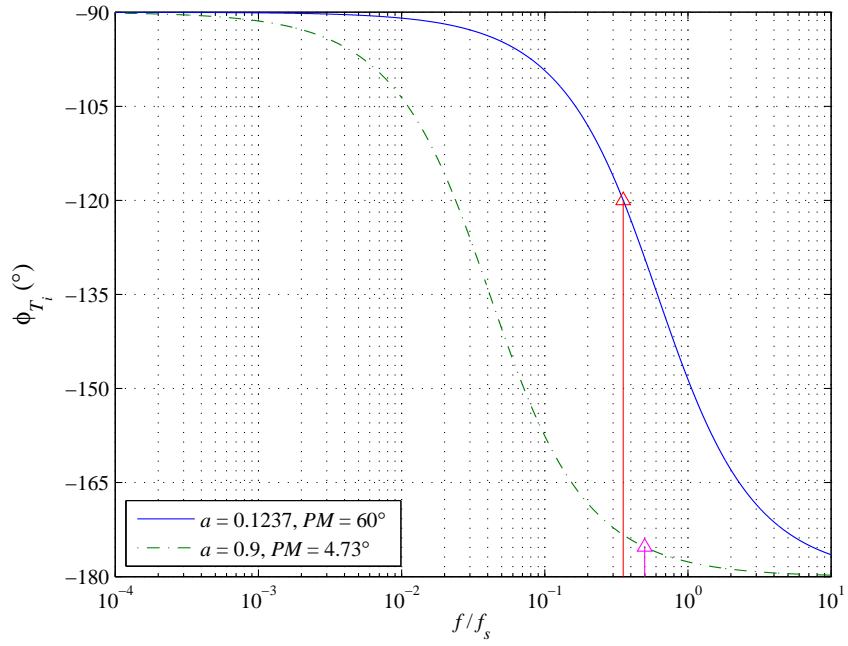


Figure 3.1: Closed-loop structure of the inner-current loop for ac components.



(a)



(b)

Figure 3.2: Bode plots of the loop gain  $T_i(s)$  at  $a = 0.1237$  and  $a = 0.9$ .



the loop gain  $T_i(s) = T_f(s)R_s$  is derived as

$$T_i(s) = T_f(s)R_s = \frac{(1+a)(e^{sT_s} - 1)}{sT_s(e^{sT_s} + a) - (1+a)(e^{sT_s} - 1)}. \quad (3.4)$$

Substituting (2.51) into (3.4), the loop gain is obtained as

$$T_i(s) \approx \frac{\pi^2 f_s^2}{s(s + \frac{\pi^2}{2} \frac{1-a}{1+a} f_s)} = \frac{\omega_h^2}{s(s + \omega_{sh})}, \quad (3.5)$$

where

$$\omega_{sh} = 2\xi_h\omega_h = \frac{\pi^2}{2} \frac{1-a}{1+a} f_s. \quad (3.6)$$

Therefore, the loop gain of the inner-current loop of peak current-mode controlled dc-dc converters is a function of the perturbation ratio  $a$  and switching frequency  $f_s$  and is independent of the converter topology. The obtained expression for loop gain matches the loop gain of inner-current loop of current-mode controlled boost converter presented in [28]. Fig. 3.2 shows the Bode plots of the loop gain at  $a = 0.1237$  and  $a = 0.9$  as a function of  $f/f_s$ . As seen from the figure, as  $a$  increases, the cross-over frequency  $f_{ci}$  increases and the phase margin  $PM$  decreases. Therefore, a lower value of  $a$  is desired to achieve a higher margin of stability.

### 3.3 Margins of Stability

The expression for loop gain given in (3.5) is a second-order function with no zeroes and a pole at the origin. The relative stability of a system is usually measured in terms of two margins of stability (a)  $GM$  (b)  $PM$ . From the Bode plots shown in Fig. 3.2, it is seen that the gain margin of the system

$$GM = \infty. \quad (3.7)$$

Therefore, the only measure of stability margin of concern for the system is its phase margin  $PM$ . In order to analyze the relative stability of the system in terms of design parameters, the analysis should be based on the phase margin  $PM$ .

### 3.4 Perturbation Ratio $a$ versus Phase Margin $PM$

Substituting  $s = j\omega$  in (3.5), we obtain

$$T_i(j\omega) = \frac{\omega_h^2}{j\omega(j\omega + \omega_{sh})} = |T_i|e^{j\phi_{Ti}}, \quad (3.8)$$

where the magnitude

$$\begin{aligned} |T_i| &= \frac{\omega_h^2}{\omega \sqrt{\omega^2 + \omega_{sh}^2}} \\ &= \frac{\omega_h^2}{\omega^2 \sqrt{1 + \left(\frac{\omega_{sh}}{\omega}\right)^2}} \\ &= \frac{1}{4} \left(\frac{f_s}{f}\right)^2 \frac{1}{\sqrt{1 + \frac{\pi^2}{16} \left(\frac{1-a}{1+a}\right)^2 \left(\frac{f_s}{f}\right)^2}} \end{aligned} \quad (3.9)$$

and the phase

$$\begin{aligned} \phi_{Ti} &= -90^\circ - \arctan\left(\frac{\omega}{\omega_{sh}}\right) \\ &= -90^\circ + \arctan\left(\frac{\omega_{sh}}{\omega}\right) - 90^\circ = -180^\circ + \arctan\left(\frac{\omega_{sh}}{\omega}\right) \\ &= -180^\circ + \arctan\left(\frac{\pi}{4} \frac{1-a}{1+a} \frac{f_s}{f}\right). \end{aligned} \quad (3.10)$$

At cross-over frequency  $f = f_{ci}$ ,

$$|T_i(f_{ci})| = 1 \quad (3.11)$$

and

$$PM = 180^\circ + \phi_{Ti(f_{ci})}. \quad (3.12)$$

Using (3.9) and (3.11),

$$|T_i(f_{ci})| = \frac{1}{4} \left(\frac{f_s}{f_{ci}}\right)^2 \frac{1}{\sqrt{1 + \frac{\pi^2}{16} \left(\frac{1-a}{1+a}\right)^2 \left(\frac{f_s}{f_{ci}}\right)^2}} = 1, \quad (3.13)$$

which gives

$$\frac{1}{4} \left(\frac{f_s}{f_{ci}}\right)^2 = \sqrt{1 + \frac{\pi^2}{16} \left(\frac{1-a}{1+a}\right)^2 \left(\frac{f_s}{f_{ci}}\right)^2} \quad (3.14)$$

and

$$\frac{1}{16} \left( \frac{f_s}{f_{ci}} \right)^4 = 1 + \frac{\pi^2}{16} \left( \frac{1-a}{1+a} \right)^2 \left( \frac{f_s}{f_{ci}} \right)^2. \quad (3.15)$$

By solving the quadratic equation

$$\frac{1}{16} \left( \frac{f_s}{f_{ci}} \right)^4 - \frac{\pi^2}{16} \left( \frac{1-a}{1+a} \right)^2 \left( \frac{f_s}{f_{ci}} \right)^2 - 1 = 0, \quad (3.16)$$

we get

$$\left( \frac{f_s}{f_{ci}} \right)^2 = \frac{\pi^2}{2} \left( \frac{1-a}{1+a} \right)^2 \left[ 1 + \sqrt{1 + \frac{64}{\pi^4} \left( \frac{1-a}{1+a} \right)^4} \right]. \quad (3.17)$$

Therefore,

$$\frac{f_s}{f_{ci}} = \frac{\pi}{\sqrt{2}} \frac{1-a}{1+a} \sqrt{1 + \sqrt{1 + \frac{64}{\pi^4} \left( \frac{1-a}{1+a} \right)^4}} \quad (3.18)$$

and

$$\begin{aligned} \frac{f_{ci}}{f_s} &= \frac{\sqrt{2}}{\pi} \frac{1+a}{1-a} \frac{1}{\sqrt{1 + \sqrt{1 + \frac{64}{\pi^4} \left( \frac{1-a}{1+a} \right)^4}}} \\ &= \frac{\sqrt{2}}{\pi} \frac{1}{\sqrt{\left( \frac{1-a}{1+a} \right)^2 + \sqrt{\left( \frac{1-a}{1+a} \right)^4 + \frac{64}{\pi^4}}}}. \end{aligned} \quad (3.19)$$

When  $a = 0$ ,  $\frac{f_{ci}}{f_s} = 0.3$  and  $a = 1$ ,  $\frac{f_{ci}}{f_s} = 0.5$ . Fig. 3.3 shows the variation of the normalized cross-over frequency  $\frac{f_{ci}}{f_s}$  as a function of the perturbation ratio  $a$ . As the perturbation ratio  $a$  increases from 0 to 1, the cross-over frequency  $f_{ci}$  increases from  $0.3f_s$  to  $0.5f_s$ .

Using (3.10), (3.12), and (3.18),

$$\begin{aligned} PM &= 180^\circ - 180^\circ + \arctan \left( \frac{\pi}{4} \frac{1-a}{1+a} \frac{f_s}{f_{ci}} \right) \\ &= \arctan \left( \frac{\pi}{4} \frac{1-a}{1+a} \frac{f_s}{f_{ci}} \right) \\ &= \arctan \left( \frac{\pi^2}{4\sqrt{2}} \left( \frac{1-a}{1+a} \right)^2 \sqrt{1 + \sqrt{1 + \frac{64}{\pi^4} \left( \frac{1-a}{1+a} \right)^4}} \right), \end{aligned} \quad (3.20)$$

which gives

$$\tan PM = \frac{\pi^2}{4\sqrt{2}} \left( \frac{1-a}{1+a} \right)^2 \sqrt{1 + \sqrt{1 + \frac{64}{\pi^4} \left( \frac{1-a}{1+a} \right)^4}}. \quad (3.21)$$

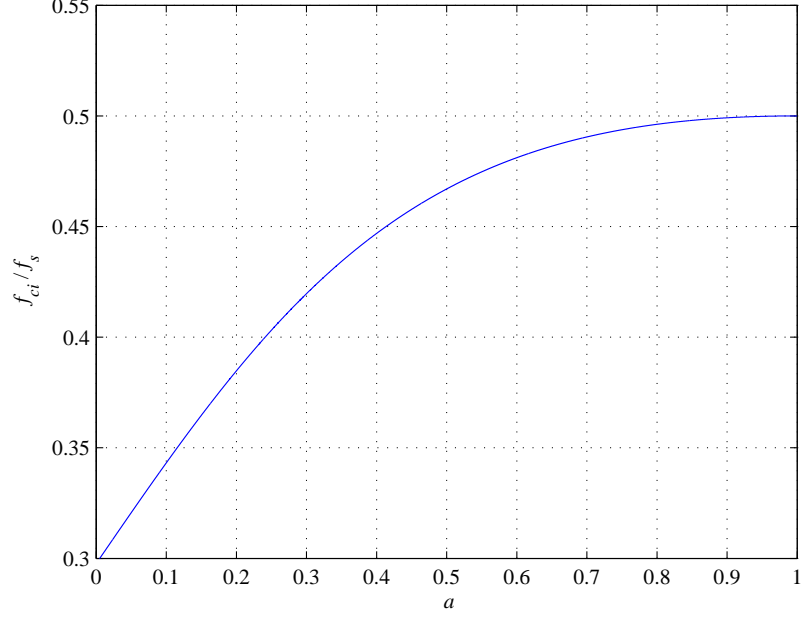


Figure 3.3: Normalized cross-over frequency  $f_{ci}/f_s$  as a function of perturbation ratio  $a$ .

Rearranging and taking squares on both sides, we get

$$\left( \left[ \frac{4\sqrt{2}}{\pi^2} \left( \frac{1+a}{1-a} \right)^2 \tan PM \right]^2 - 1 \right)^2 = 1 + \frac{64}{\pi^4} \left( \frac{1+a}{1-a} \right)^4, \quad (3.22)$$

which gives

$$\left[ \frac{32}{\pi^4} \left( \frac{1+a}{1-a} \right)^4 \tan^2 PM - 1 \right]^2 = 1 + \frac{64}{\pi^4} \left( \frac{1+a}{1-a} \right)^4. \quad (3.23)$$

Expanding (3.23) results in

$$\left( \frac{32}{\pi^4} \right)^2 \left( \frac{1+a}{1-a} \right)^8 \tan^4 PM - \frac{64}{\pi^4} \left( \frac{1+a}{1-a} \right)^4 \tan^2 PM + 1 = 1 + \frac{64}{\pi^4} \left( \frac{1+a}{1-a} \right)^4, \quad (3.24)$$

which simplifies into

$$\frac{16}{\pi^4} \left( \frac{1+a}{1-a} \right)^4 \tan^4 PM - \tan^2 PM = 1 \quad (3.25)$$

and gives

$$\left( \frac{1+a}{1-a} \right)^4 = \left( \frac{\pi}{2} \right)^4 \frac{1 + \tan^2 PM}{\tan^4 PM}. \quad (3.26)$$

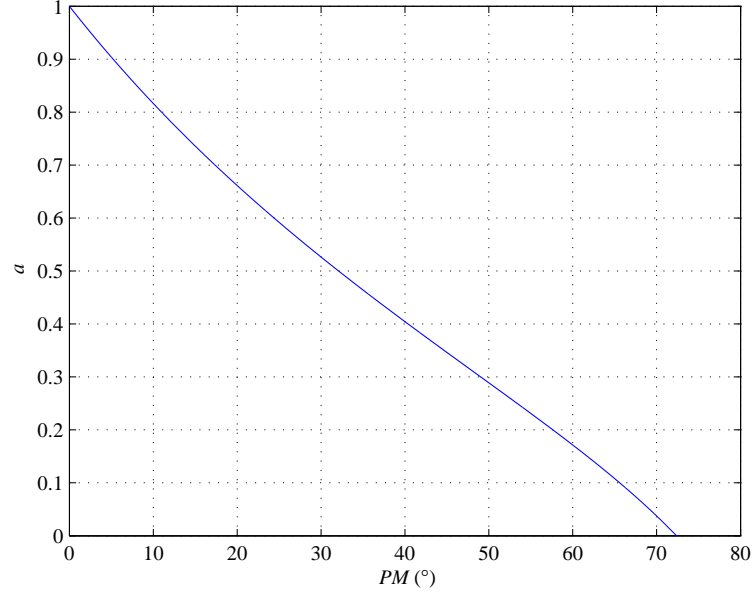


Figure 3.4: Perturbation ratio  $a$  versus phase margin  $PM$ .

Therefore, the perturbation ratio  $a$  as a function of the phase margin  $PM$  is obtained as

$$a = \frac{\sqrt[4]{1 + \tan^2 PM} - \frac{2}{\pi} \tan PM}{\sqrt[4]{1 + \tan^2 PM} + \frac{2}{\pi} \tan PM}. \quad (3.27)$$

When  $PM = 0^\circ$ ,  $a = 1$ . Fig. 3.4 shows the variation of perturbation ratio  $a$  as a function of phase margin  $PM$ . At  $PM = 45^\circ$  and  $60^\circ$ ,  $a = 0.3027$  and  $0.1237$ , respectively. A low value of  $a$  is desired to obtain a reasonable margin of stability in terms of phase margin.

## 4 Peak Current-Mode Control without Slope Compensation

It is commonly believed that, for applications with duty cycle  $D < 0.5$ , peak current-mode control with slope compensation is sufficient [5]-[33]. In Sections 4.1-4.6, the boundary between stable and unstable operations as well as the relative stability of the system will be analyzed, expressions for the control current required by buck, boost, and buck-boost converters in CCM operation will be derived, and simulation results and experimental results to support the proposed theory will be presented.

### 4.1 Boundary Between Stable and Unstable Operations

The perturbation ratio  $a$  of the peak current-mode controlled converters without slope compensation operating in CCM was derived in Section 2.2.2 as

$$a = \frac{\Delta i_{Ln}}{\Delta i_{L(n-1)}} = \frac{D}{1-D}. \quad (4.1)$$

Using the stability conditions given in (2.3)-(2.7)

- for a stable system,  $a < 1$

$$\frac{D}{1-D} < 1 \implies D < 0.5, \quad (4.2)$$

- for a marginally stable system,  $a = 1$

$$\frac{D}{1-D} = 1 \implies D = 0.5, \quad (4.3)$$

- and for an unstable system,  $a > 1$

$$\frac{D}{1-D} > 1 \implies D > 0.5. \quad (4.4)$$

Therefore, the inner-current loop of the peak current-mode controlled converters without slope compensation is stable for operations at  $D < 0.5$ . But the inner loop has

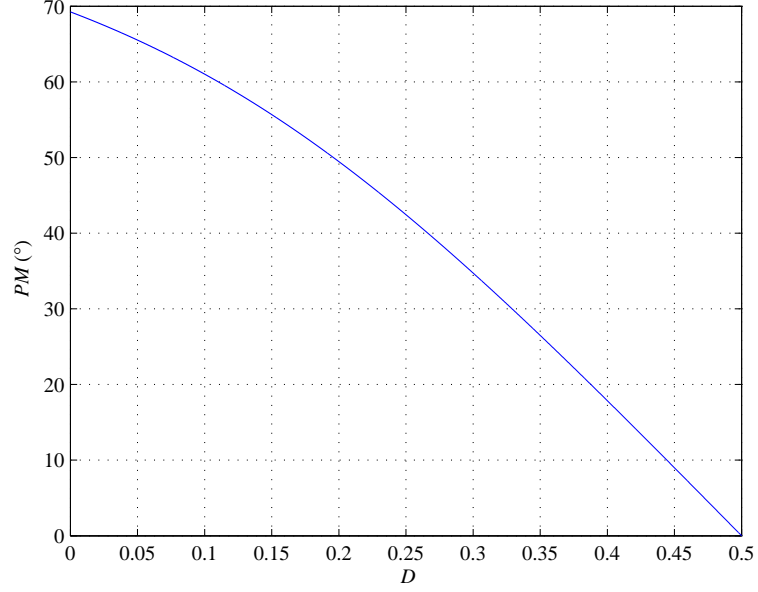


Figure 4.1: Phase margin  $PM$  as a function of duty cycle  $D$  for peak current-mode control without compensation.

to be sufficiently stable to ensure proper operation of the inner loop. Therefore, the relative stability of the inner-current loop of peak current-mode controlled converters without slope compensation has to be analyzed.

## 4.2 Relative Stability

The relative stability of peak current-mode controlled systems was analyzed in terms of the perturbation ratio and the phase margin in Section 3.4. Substituting (3.27) into (4.1), we get

$$\frac{\sqrt[4]{1 + \tan^2 PM} - \frac{2}{\pi} \tan PM}{\sqrt[4]{1 + \tan^2 PM} + \frac{2}{\pi} \tan PM} = \frac{D}{1 - D}, \quad (4.5)$$

which gives

$$\sqrt[4]{1 + \tan^2 PM} - \frac{2}{\pi} \tan PM = 2D \sqrt[4]{1 + \tan^2 PM}. \quad (4.6)$$

Therefore, the duty cycle  $D$  as a function of phase margin  $PM$  is obtained as

$$D = 0.5 - \frac{\tan PM}{\pi \sqrt[4]{1 + \tan^2 PM}}. \quad (4.7)$$

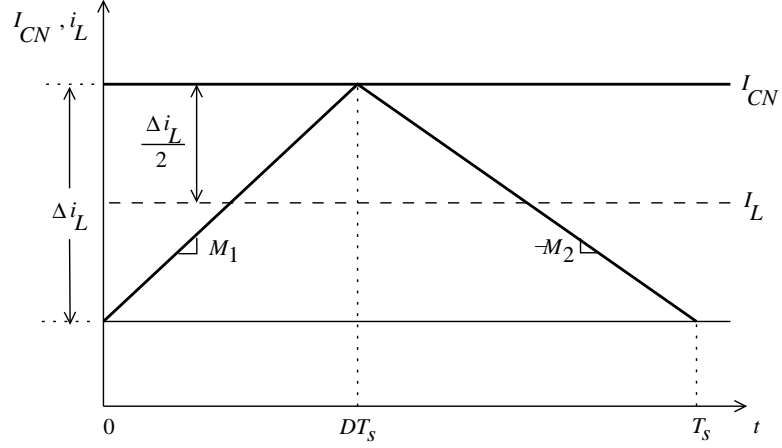


Figure 4.2: Steady-state inductor current  $i_L$  waveform and control current  $I_{CN}$  without slope compensation.

The phase margin  $PM$  as a function of duty cycle  $D$  is derived as

$$PM = \arctan \left[ \frac{\pi^2(0.5 - D)^2}{\sqrt{2}} \sqrt{1 + \sqrt{1 + \frac{4}{\pi^4(0.5 - D)^4}}} \right]. \quad (4.8)$$

As shown in (4.7), for current-mode controlled systems without slope compensation, while the inner-loop is stable for  $0 \leq D \leq 0.5$ , duty cycle values with sufficient degree of stability margin are much less than 0.5. Fig. 4.1 shows the phase margin as a function of duty cycle for any converter with current-mode control without slope compensation. At  $D = 0.5$ ,  $PM = 0^\circ$ . As the duty cycle  $D$  decreases from 0.5 to 0, the phase margin  $PM$  increases from  $0^\circ$  to  $69.2^\circ$ . The phase margin  $PM \geq 60^\circ$  for  $0 < D < 0.1102$ .

### 4.3 General Equation for Control Current Level Without Slope Compensation

From Fig. 4.2, the general equation for the dc level of control current without slope compensation for all second-order dc-dc converters is

$$I_{CN} = I_L + \frac{\Delta i_L}{2} = I_L + \frac{M_1 D}{2f_s}. \quad (4.9)$$

Thus, the required control current without compensation is dependent on the average value of inductor current  $I_L$ , the on-slope of the inductor current  $M_1$ , the duty cycle



$D$ , and the switching frequency  $f_s$ .

#### 4.3.1 Buck Converter

Let  $V_O$ ,  $V_I$ , and  $L$  be the output voltage, the input voltage, and the inductance, respectively. The dc voltage transfer function of the buck converter is given by

$$M_{VDC} = \frac{V_O}{V_I} = D, \quad (4.10)$$

the average inductor current is

$$I_L = I_O = \frac{V_O}{R_L}, \quad (4.11)$$

and the on-slope of the inductor current waveform is

$$M_1 = \frac{V_I - V_O}{L} = \frac{V_O(1 - D)}{DL}. \quad (4.12)$$

Substituting (4.10)-(4.12) into (4.9), the dc control current required for a buck converter without slope compensation is

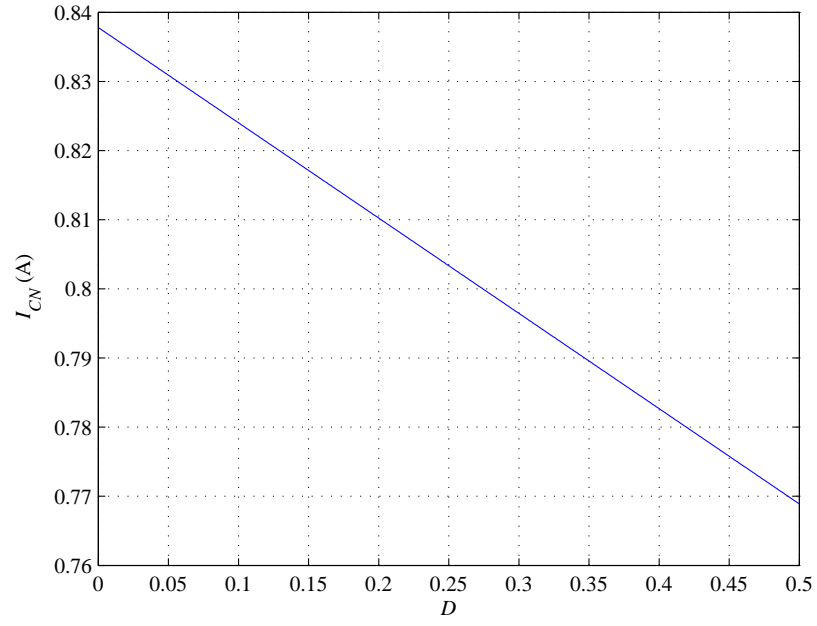
$$I_{CN} = I_O + \frac{V_O(1 - D)}{2f_s L}. \quad (4.13)$$

Fig. 4.3(a) shows the dc control current as a function of duty cycle  $D$  for the selected buck converter with  $V_O = 7$  V,  $I_O = 0.7$  A,  $L = 254$   $\mu$ H, and  $f_s = 100$  kHz. As  $D$  increases, the on-slope  $M_1$  of the inductor current decreases and thereby the dc level of control current required decreases.

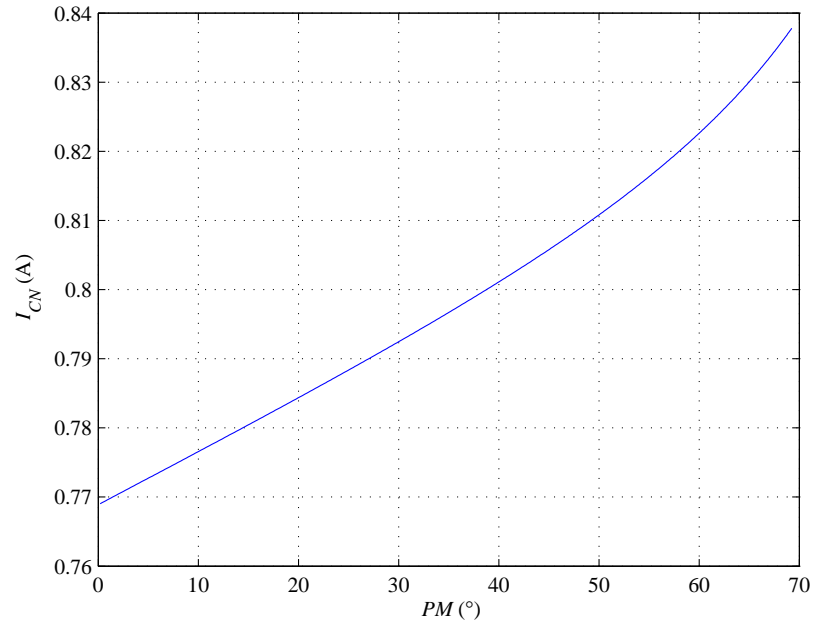
Substitution of (4.7) into (4.13) produces the relationship between the control current and the phase margin given by

$$I_{CN} = I_O + \frac{V_O}{4f_s L} \left[ 1 + \frac{2 \tan PM}{\pi \sqrt[4]{1 + \tan^2 PM}} \right]. \quad (4.14)$$

The control current as a function of the phase margin is shown in Fig. 4.3(b). The required control current increases with increase in the phase margin.



(a)



(b)

Figure 4.3: DC control current  $I_{CN}$  as functions of duty cycle  $D$  and phase margin  $PM$  for buck converter with  $V_O = 7$  V,  $I_O = 0.7$  A,  $L = 254$   $\mu$ H, and  $f_s = 100$  kHz. (a)  $I_{CN}$  versus  $D$ . (b)  $I_{CN}$  versus  $PM$ .

### 4.3.2 Boost Converter

For the boost converter, the dc voltage transfer function is

$$M_{VDC} = \frac{V_O}{V_I} = \frac{1}{1-D}, \quad (4.15)$$

the average inductor current is

$$I_L = \frac{I_O}{1-D} = \frac{V_O}{R_L(1-D)}, \quad (4.16)$$

and the on-slope of the inductor current waveform is

$$M_1 = \frac{V_I}{L} = \frac{V_O(1-D)}{L}. \quad (4.17)$$

By substituting (4.15)-(4.17) into (4.9), the dc control current level without slope compensation for the boost converter is

$$I_{CN} = \frac{I_O}{1-D} + \frac{V_O(1-D)D}{2f_s L}. \quad (4.18)$$

Fig. 4.4(a) shows the variation of control current without compensation for a boost converter with  $V_O = 400$  V,  $I_O = 0.225$  A,  $L = 20$  mH, and  $f_s = 100$  kHz as a function of duty cycle. As the duty cycle increases, the control current required increases.

Substituting (4.7) into (4.18), the control current as a function of phase margin is obtained as

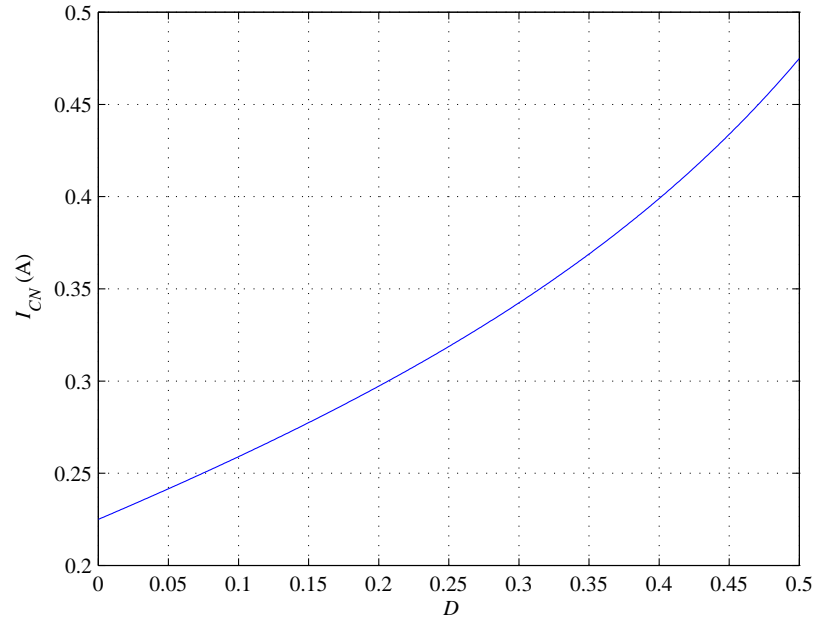
$$I_{CN} = \frac{I_O}{\left[1 + \frac{2 \tan PM}{\pi^4 \sqrt{1 + \tan^2 PM}}\right]} + \frac{V_O}{8f_s L} \left[1 - \frac{4 \tan^2 PM}{\pi^2 \sqrt{1 + \tan^2 PM}}\right] \quad (4.19)$$

As shown in Fig. 4.4(b), the control current decreases with increase in phase margin.

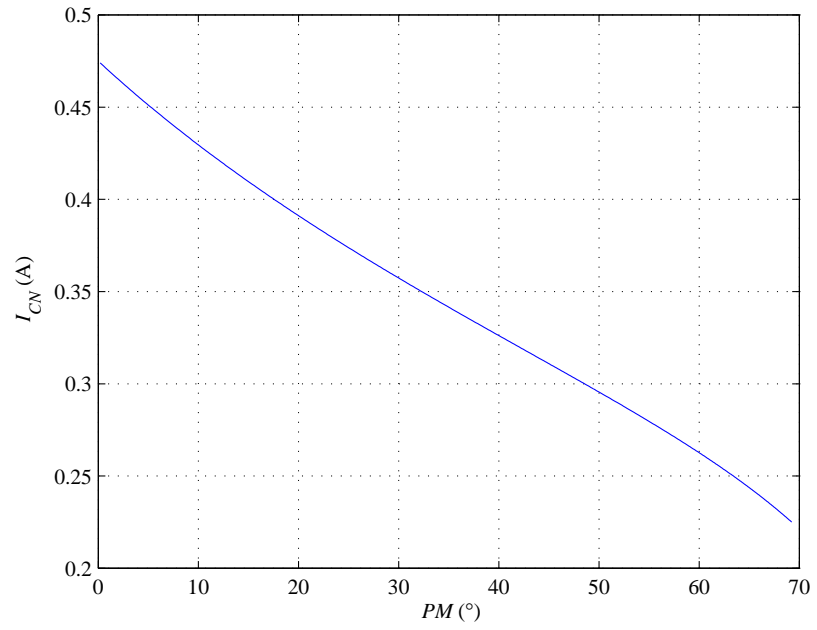
### 4.3.3 Buck-Boost Converter

For the buck-boost converter, the dc voltage transfer function, the average inductor current, and the on-slope of the inductor current waveform are respectively given by

$$M_{VDC} = \frac{V_O}{V_I} = \frac{D}{1-D}, \quad (4.20)$$

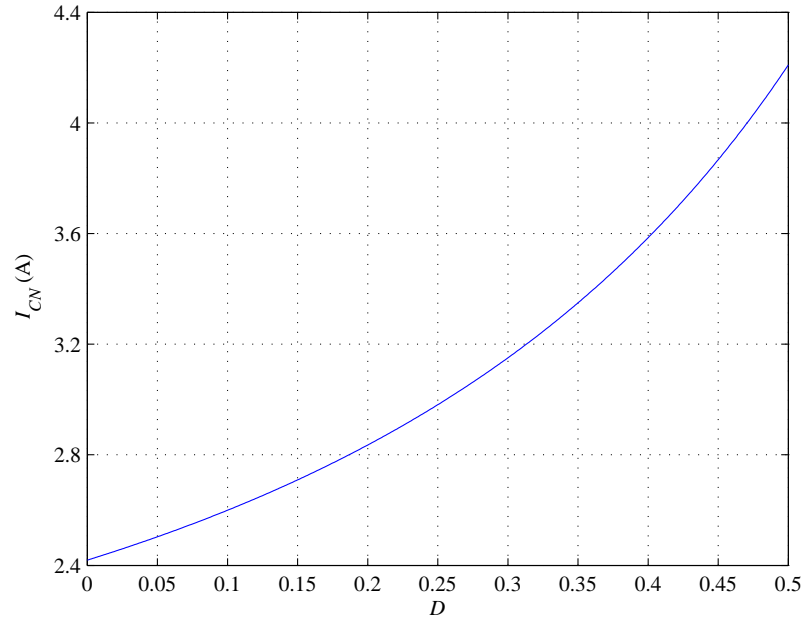


(a)

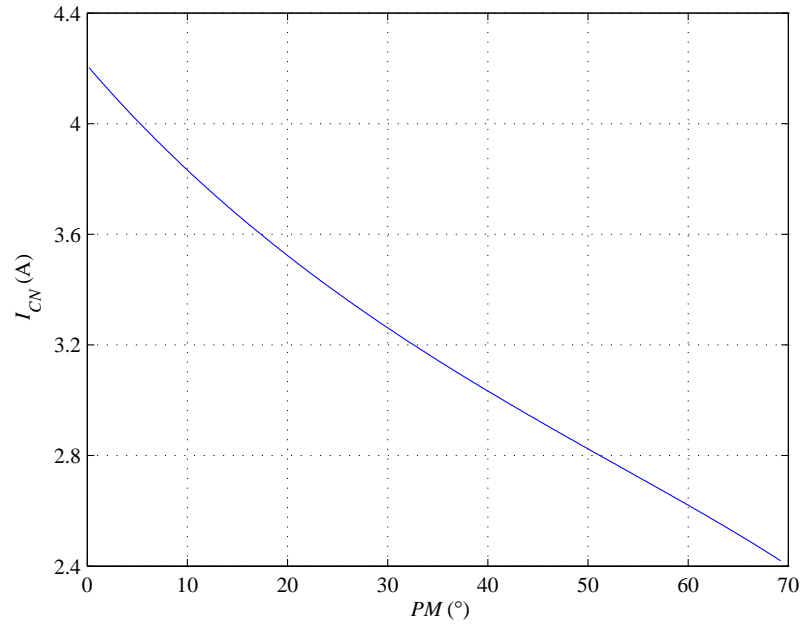


(b)

Figure 4.4: DC control current  $I_{CN}$  as functions of duty cycle  $D$  and phase margin  $PM$  for boost converter with  $V_O = 400$  V,  $I_O = 0.225$  A,  $L = 20$  mH, and  $f_s = 100$  kHz. (a)  $I_{CN}$  versus  $D$ . (b)  $I_{CN}$  versus  $PM$ .



(a)



(b)

Figure 4.5: DC control current  $I_{CN}$  as functions of duty cycle  $D$  and phase margin  $PM$  for buck-boost converter with  $V_O = 28$  V,  $I_O = 2$  A,  $L = 334$   $\mu$ H, and  $f_s = 100$  kHz. (a)  $I_{CN}$  versus  $D$ . (b)  $I_{CN}$  versus  $PM$ .

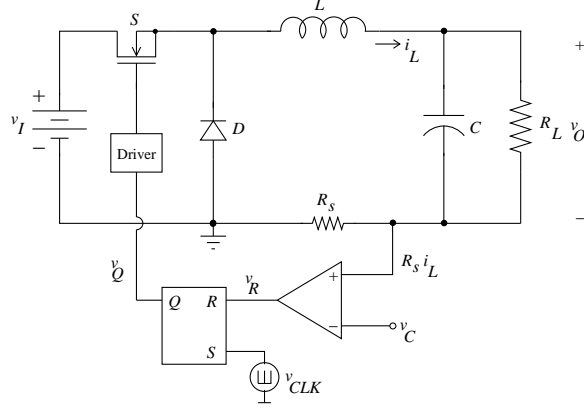


Figure 4.6: Peak current-mode controlled PWM dc-dc buck converter with inner-current loop only.

$$I_L = \frac{I_O}{1 - D} = \frac{V_O}{R_L(1 - D)}, \quad (4.21)$$

and

$$M_1 = \frac{V_I}{L} = \frac{V_O(1 - D)}{DL}. \quad (4.22)$$

The expression for dc control current without slope compensation is obtained as

$$I_{CN} = \frac{I_O}{1 - D} + \frac{V_O(1 - D)}{2f_s L}. \quad (4.23)$$

The required control voltage as a function of the duty cycle for the buck-boost converter with  $V_O = 28$  V,  $I_O = 2$  A,  $L = 334$   $\mu$ H, and  $f_s = 100$  kHz is plotted in Fig. 4.5(a). As the duty cycle increases, the control current required increases non-linearly.

The control current as a function of the phase margin is obtained as

$$I_{CN} = \frac{I_O}{\left[1 + \frac{2 \tan PM}{\pi^4 \sqrt{1 + \tan^2 PM}}\right]} + \frac{V_O}{4f_s L} \left[1 + \frac{2 \tan PM}{\pi^4 \sqrt{1 + \tan^2 PM}}\right], \quad (4.24)$$

by substituting (4.7) into (4.23). Fig. 4.5(b) depicts the required control current for the selected buck-boost converter as a function of phase margin. As the phase margin increases, the control current decreases.

Table 4.1:  $I_{CN}$  and  $V_{CN}$  required at specified values of  $V_I$  and  $R_s = 1 \Omega$  to obtain  $V_O = 7 \text{ V}$ .

$V_I \text{ (V)}$	$D$	$I_{CN} \text{ (A)}$	$V_{CN} = R_s I_{CN} \text{ V}$
70	0.1	0.824	0.824
46.67	0.15	0.8171	0.8171
35	0.2	0.8102	0.8102
28	0.25	0.8034	0.8034
23.33	0.3	0.7965	0.7965
20	0.35	0.7896	0.7896
17.5	0.4	0.7827	0.7827
15.56	0.45	0.7758	0.7758
14	0.5	0.7689	0.7689

#### 4.4 Design Example

A peak current-mode controlled PWM dc-dc buck converter without slope compensation, with inner current loop only is shown in Fig. 4.6. The selected buck converter has  $14 \text{ V} \leq V_I \leq 70 \text{ V}$ ,  $V_O = 7 \text{ V}$ ,  $I_O = 0.7 \text{ A}$ ,  $L = 254 \mu\text{H}$  and  $f_s = 100 \text{ kHz}$ . The minimum and maximum values of duty cycle are, respectively,

$$D_{min} = \frac{V_O}{V_{I_{max}}} = \frac{7}{70} = 0.1 \quad (4.25)$$

and

$$D_{max} = \frac{V_O}{V_{I_{min}}} = \frac{7}{14} = 0.5. \quad (4.26)$$

Using (4.13), the minimum and maximum values of required control current are obtained as

$$I_{CNmin} = I_{CN} \Big|_{D=D_{max}} = I_O + \frac{V_O(1 - D_{max})}{2f_s L} = 0.7 + \frac{7(1 - 0.5)}{2 \times 10^5 \times 254 \times 10^{-6}} = 0.7689 \quad (4.27)$$

and

$$I_{CNmax} = I_{CN} \Big|_{D=D_{min}} = I_O + \frac{V_O(1 - D_{min})}{2f_s L} = 0.7 + \frac{7(1 - 0.1)}{2 \times 10^5 \times 254 \times 10^{-6}} = 0.824, \quad (4.28)$$

respectively. Therefore, the required control current range for the full range of operation is  $I_{CN} = \langle 0.7689, 0.824 \rangle$ . Table 4.4 shows the calculated values of required control current  $I_{CN}$  to obtain the specified  $D$  at  $V_I$ , and  $V_O = 7$  V and required control voltage  $V_{CN} = R_s I_{CN}$  with  $R_s = 1 \Omega$ .

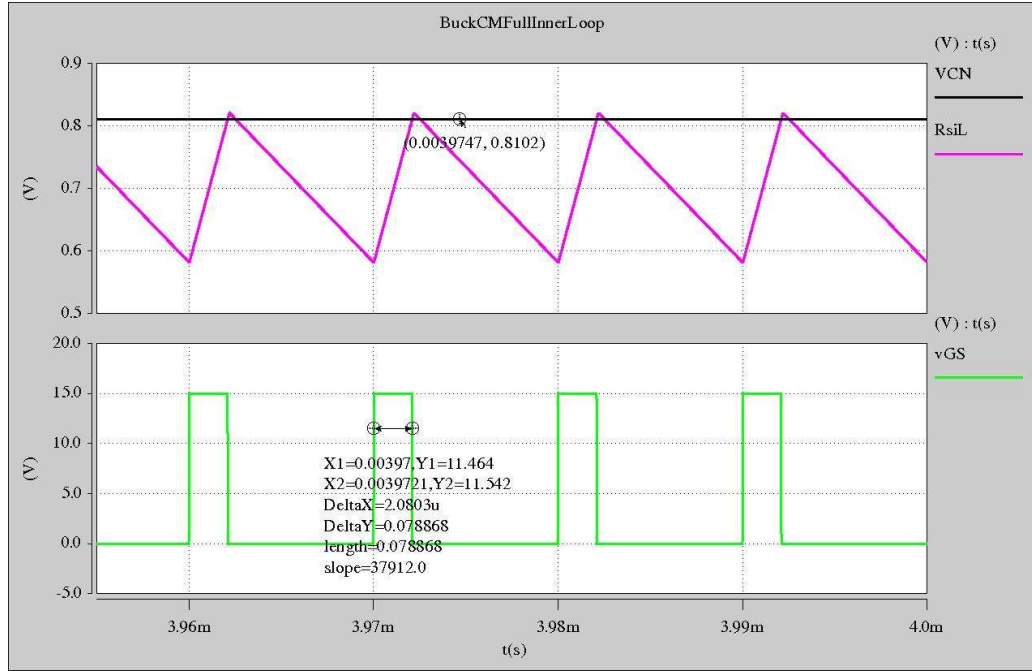
## 4.5 Simulation Results

The PWM dc-dc buck converter shown in Fig. 4.6 was simulated using Saber Sketch. Control voltage, sensed inductor current, and MOSFET gate-to-source voltage waveforms at specified input voltages to obtain  $V_O = 7$  V are shown in Figs. 4.7-4.8. The control current and control voltage values corresponding to selected duty cycle values was obtained from Table 4.4. Fig. 4.7(a) and (b) shows the waveforms corresponding to duty cycles 0.21 and 0.37. In Fig. 4.8(a), waveforms correspond to  $D = 0.54$  and as seen from the figure, the system has entered the unstable region of operation and the inductor current has started to assumed a ‘M’ shape. Fig. 4.8(b) shows the waveforms for  $V_I = 12$  V, which shows that the system is unstable and is exhibiting period doubling. A comparison of theoretical and Saber simulation results is shown in Fig. 4.9. The simulation results agreed very well with the theoretical prediction values.

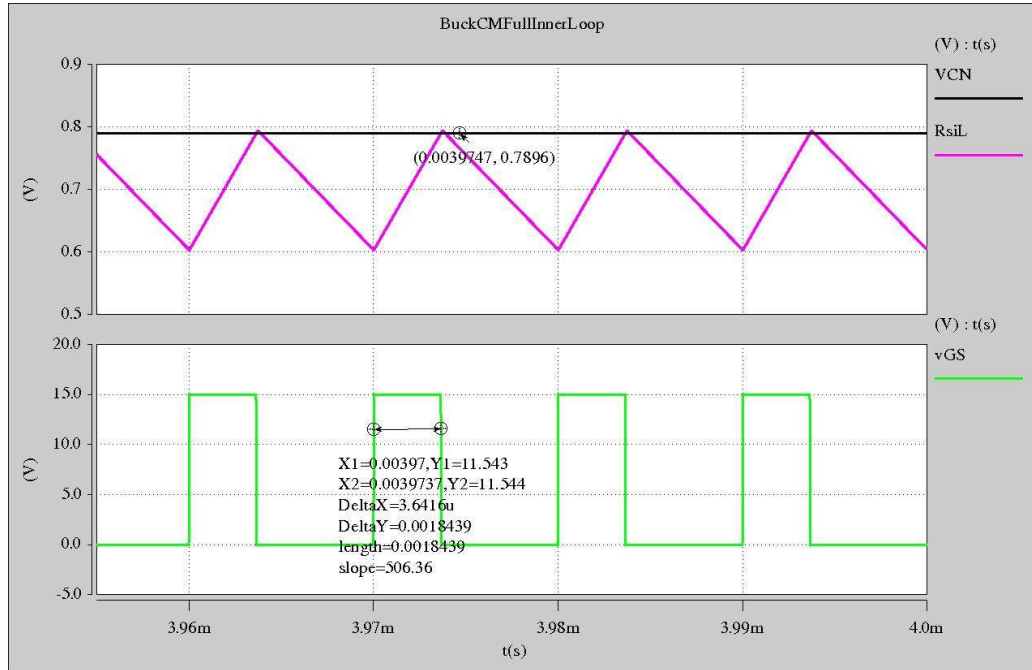
## 4.6 Experimental Results

The PWM dc-dc buck converter shown in Fig. 4.6 was set up and the results obtained in Section 4.3.1 were verified experimentally. The experimental setup had the following specifications: input voltage  $14 \text{ V} \leq V_I \leq 35 \text{ V}$ , output voltage  $V_O = 7 \text{ V}$ , output current  $I_O = 0.7 \text{ A}$ , inductance  $L = 254 \mu\text{H}$ , capacitance  $C = 68 \mu\text{F}$ , load resistance  $R_L = 10 \Omega$ , sense resistor  $R_s = 1 \Omega$  and switching frequency  $f_s = 100 \text{ kHz}$ . Using (4.10), the range of duty cycle required is  $0.2 \leq D \leq 0.5$ . The switching components chosen were: IRF530 power MOSFET with the ratings  $B_{VDS} = 100 \text{ V}$ ,  $I_D = 14 \text{ A}$ ,



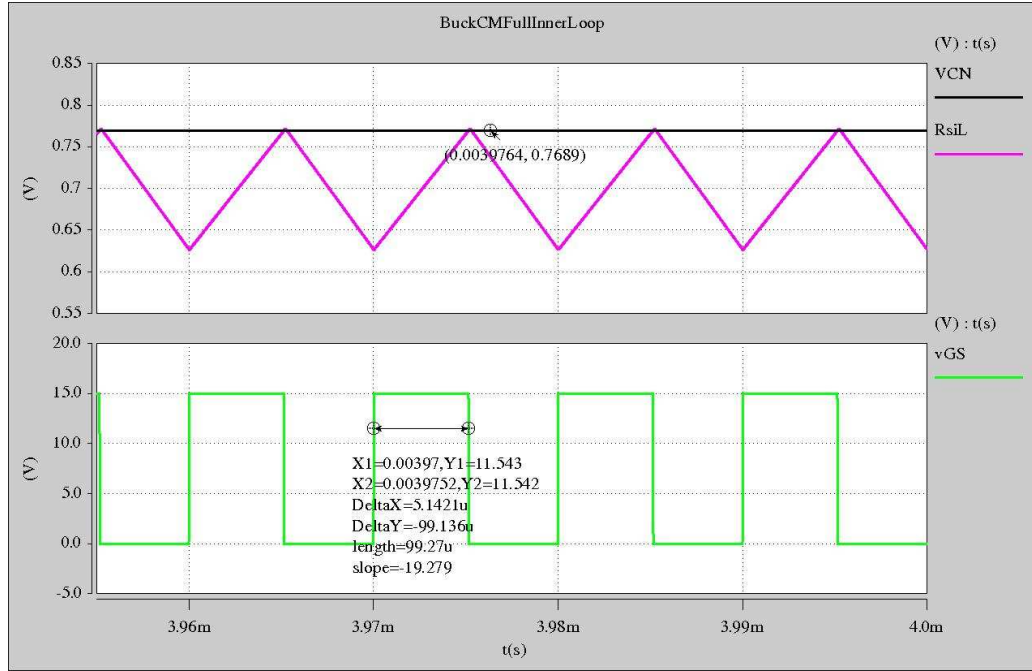


(a)

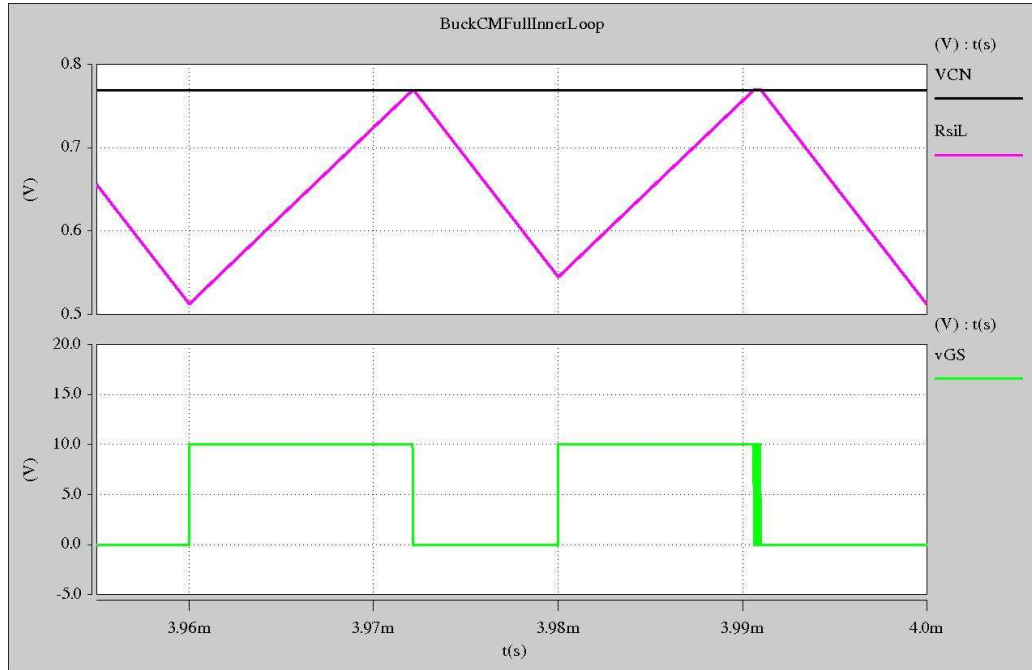


(b)

Figure 4.7: Control voltage  $V_{CN}$ , sensed inductor current  $R_{siL}$ , and MOSFET gate-to-source voltage  $V_{GS}$  waveforms obtained using Saber simulations. (a)  $V_I = 35$  V and  $V_{CN} = R_s I_{CN} = 0.8102$  V. (b)  $V_I = 20$  V and  $V_{CN} = R_s I_{CN} = 0.7896$  V.



(a)



(b)

Figure 4.8: Control voltage  $V_{CN}$ , sensed inductor current  $R_{siL}$ , and MOSFET gate-to-source voltage  $V_{GS}$  waveforms obtained using Saber simulations. (a)  $V_I = 14$  V and  $V_{CN} = R_s I_{CN} = 0.7689$  V. (b)  $V_I = 12$  V and  $V_{CN} = R_s I_{CN} = 0.7689$  V.

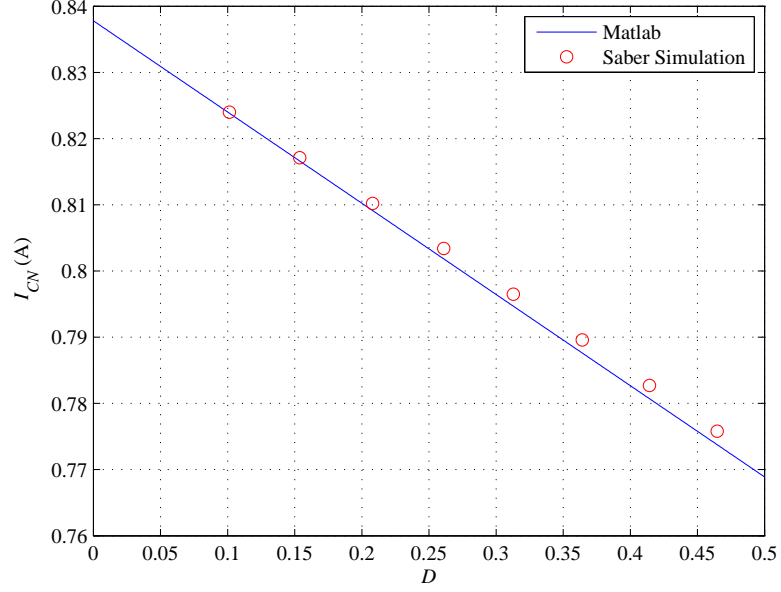


Figure 4.9: Comparison of theoretical and Saber simulation results.

and  $r_{DS} = 0.16 \, \Omega$  and MUR820 power diode with  $BV = 200 \, \text{V}$ ,  $V_F = 0.975 \, \text{V}$  and  $R_F = 0.01 \, \Omega$ . The experimental setup to measure duty cycle at given values of control voltage is shown in Fig. 4.10. The sensed inductor ripple current is measured using a wide-band current transformer manufactured by Pearson Electronics and the gate-to-source voltage is measured by Probe Master differential probe.

The dc control current as a function of duty cycle obtained theoretically and experimentally are compared in Fig. 4.11(a). The values of  $I_{CN}$  required for specified values of  $D$  were obtained from Fig. 4.3(a). The control voltage  $V_{CN} = R_s I_{CN}$  was applied to the experimental setup and the resultant values of  $D$  have been noted. Fig. 4.11(a) shows the values of  $D$  obtained for the respective values of  $V_{CN}$  in comparison with Fig. 4.3(a). The theoretical and experimental values of  $V_{CN}$  with respect to  $V_I$  are shown in Fig. 4.11(b). The difference between the experimental results and the predicted values can be accounted by the efficiency of the circuit. The value of output voltage obtained was  $V_O = 6.6 \, \text{V}$ .

Fig. 4.12 shows the sensed inductor ripple current  $R_s \Delta i_L$  and gate-to-source volt-

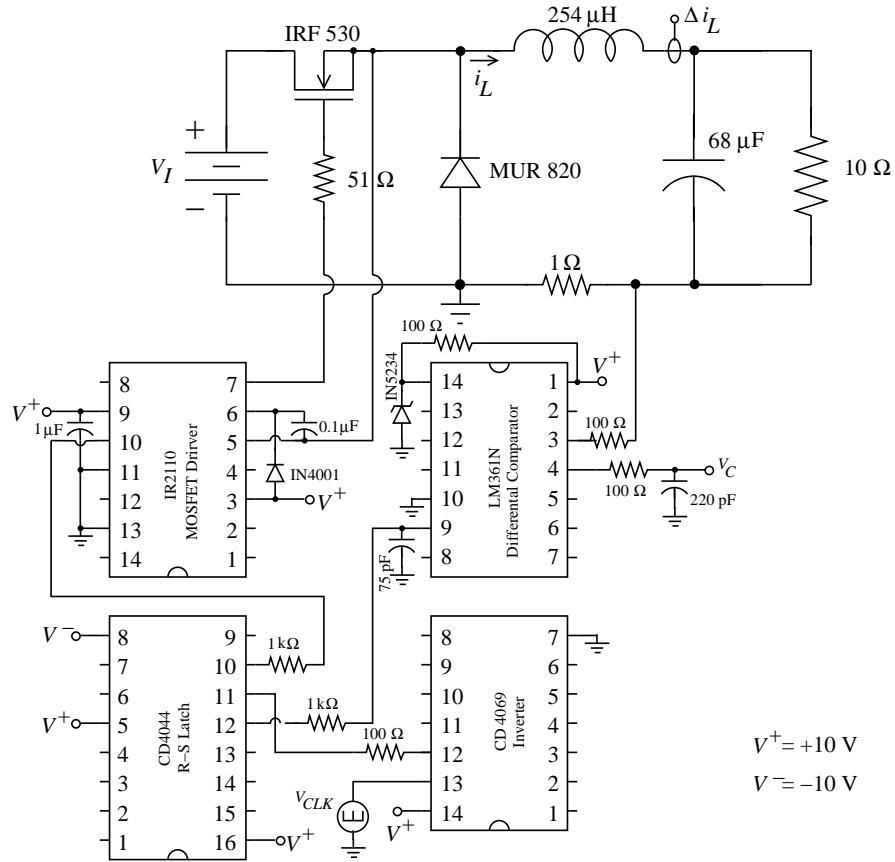
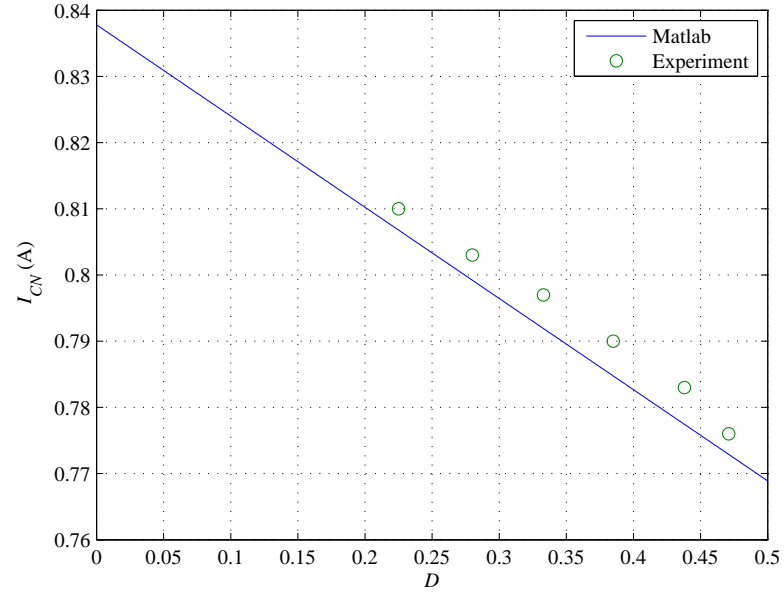


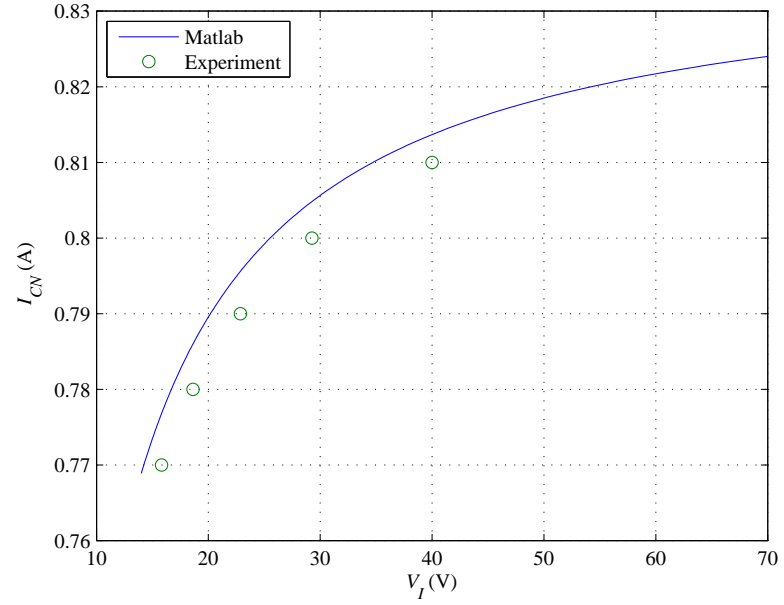
Figure 4.10: Experimental setup to measure duty cycle at given values of control voltage.

age waveforms  $V_{GS}$  at  $V_{Imax} = 35$  V and  $V_{CN} = 0.81$  V. It is seen from figure, the resultant duty cycle is 0.23 and the system is stable with a phase margin of  $49^\circ$ . In Fig. 4.13, the waveforms with  $D = 0.385$ , and  $PM = 21^\circ$  are obtained at  $V_{CN} = 0.79$  V and  $V_I = 20$  V. The waveforms corresponding to  $V_I = 15.56$  V and  $V_{CN} = 0.776$  V are shown in Fig. 4.14. The duty cycle obtained was  $D = 0.471$  and it is seen that the system has already entered the unstable region. Thus, the inner-loop has become unstable at  $V_I = 15.56$  V, while the specified minimum value of input voltage was  $V_{Imin} = 14$  V. Therefore, the input voltage range where the system is stable was reduced from  $14 \text{ V} \leq V_I \leq 35 \text{ V}$  to  $15.56 \text{ V} \leq V_I \leq 35 \text{ V}$ .

Fig. 4.15(a)-(c) shows the transition of the system to the unstable region causing period doubling with  $V_{CN} = 0.769$  V and  $V_I = 15$  V, 14 V, and 12.56 V, respectively.



(a)



(b)

Figure 4.11: Experimental and theoretical values of DC control current  $I_{CN}$  as functions of duty cycle  $D$  and input voltage  $V_I$  for buck converter with  $V_O = 7$  V,  $I_O = 0.7$  A,  $L = 254$   $\mu$ H,  $f_s = 100$  kHz, and  $R_s = 1$   $\Omega$ . (a)  $I_{CN}$  versus  $D$ . (b)  $I_{CN}$  versus  $V_I$ .

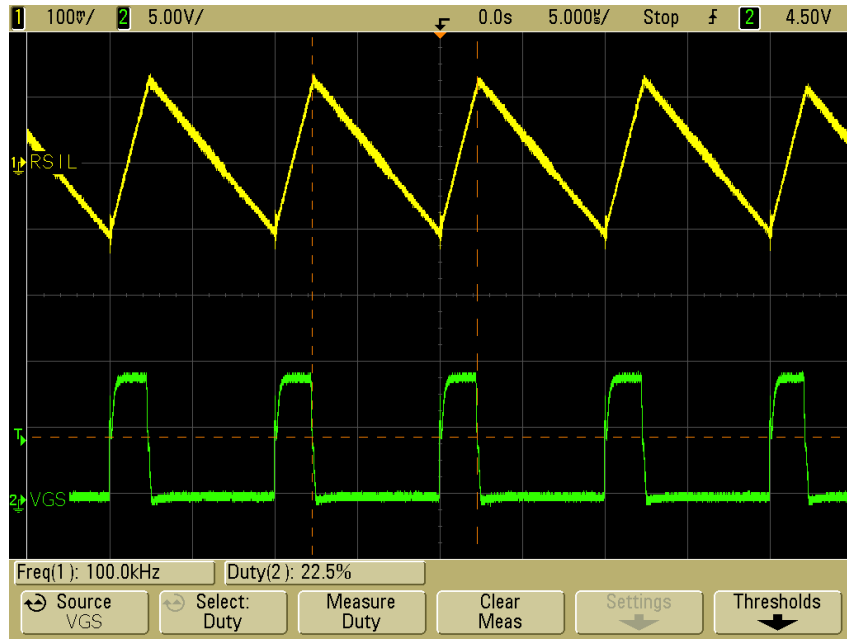


Figure 4.12: Sensed inductor ripple current  $R_s(i_L - I_L)$  and MOSFET gate-to-source  $V_{GS}$  voltage waveforms from the experimental set-up with  $V_I = 35$  V and  $V_{CN} = R_s I_{CN} = 0.81$  V.

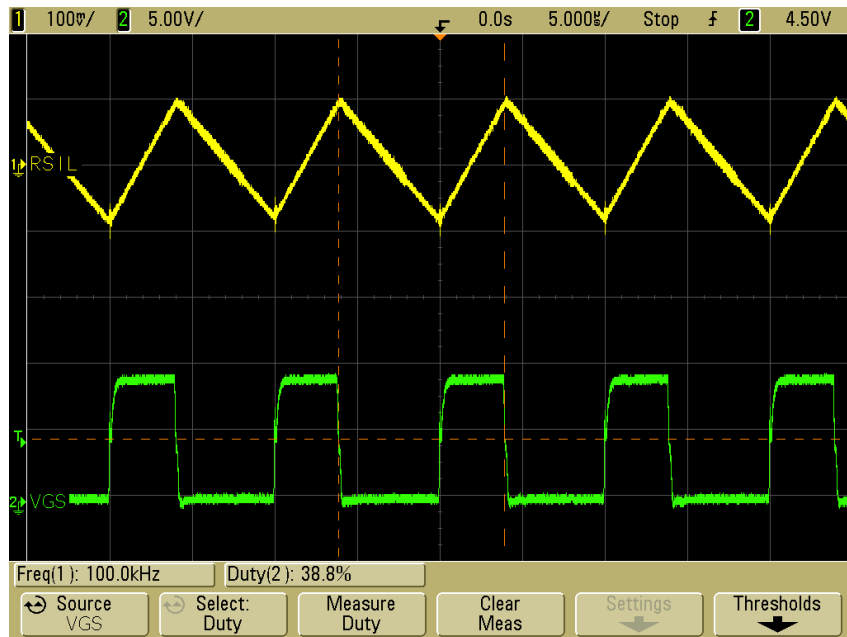


Figure 4.13: Sensed inductor ripple current  $R_s(i_L - I_L)$  and MOSFET gate-to-source voltage waveforms from the experimental set-up with  $V_I = 20$  V and  $V_{CN} = R_s I_{CN} = 0.79$  V.

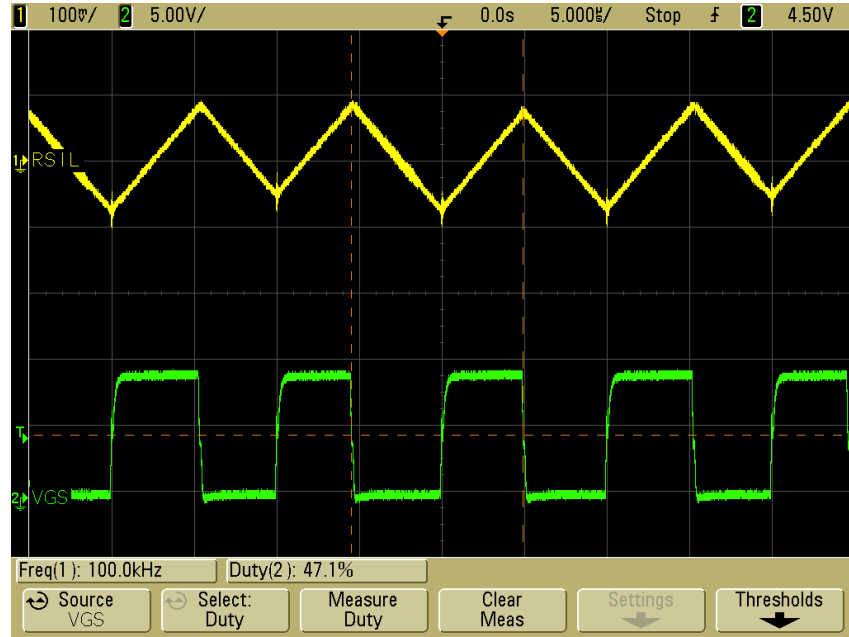
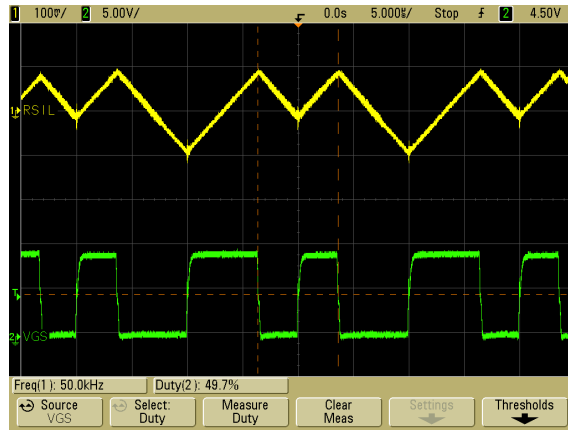
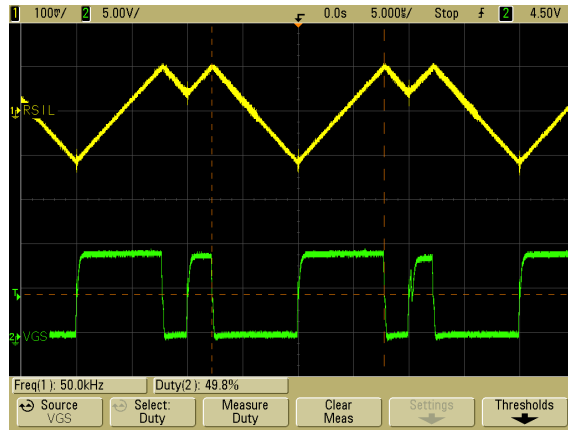


Figure 4.14: Sensed inductor ripple current  $R_s(i_L - I_L)$  and MOSFET gate-to-source voltage  $V_{GS}$  waveforms from the experimental set-up with  $V_I = 15.56$  V and  $V_{CN} = R_s I_{CN} = 0.776$  V.

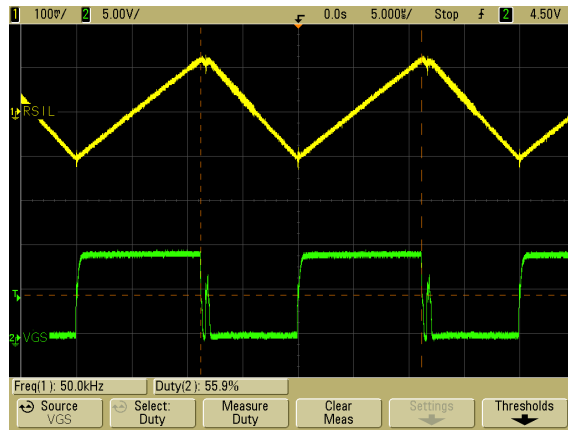
Thus, the system was unstable at  $D \geq 0.5$  as expected for uncompensated current-mode controlled converters. However, the inner-loop entered the unstable region within the specified input voltage range, which is undesirable.



(a)



(b)



(c)

Figure 4.15: Sensed inductor ripple current  $R_s(i_L - I_L)$  and MOSFET gate-to-source voltage  $V_{GS}$  waveforms showing transformation from stable to unstable operation. (a)  $V_I = 15$  V and  $V_{CN} = R_s I_{CN} = 0.769$  V. (b)  $V_I = 14$  V and  $V_{CN} = R_s I_{CN} = 0.769$  V. (c)  $V_I = 12.56$  V and  $V_{CN} = R_s I_{CN} = 0.769$  V.



## 5 Peak Current-Mode Control with Slope Compensation

As already mentioned, peak current-mode control without slope compensation is unstable for duty cycle values  $D > 0.5$ . Peak current-mode control with slope compensation could be employed in order to ensure a stable operation for duty cycle values greater than 0.5.

### 5.1 Boundary Between Stable and Unstable Regions of Operation

For the peak current-mode controlled converters with slope compensation operating in CCM, the perturbation ratio  $a$  was derived in Section 2.2.3 as

$$a = \frac{\Delta i_{Ln}}{\Delta i_{L(n-1)}} = \frac{\frac{D}{1-D} - \frac{M_3}{M_1}}{1 + \frac{M_3}{M_1}}. \quad (5.1)$$

For marginally stable systems, the perturbation ratio  $a = 1$ . Therefore, at  $D = D_{max}$ ,  $M_1 = M_{1min} = M_1 \Big|_{D_{max}}$ , and  $M_3 = M_{3cr}$ ,

$$a = \frac{\frac{D_{max}}{1-D_{max}} - \frac{M_{3cr}}{M_{1min}}}{1 + \frac{M_{3cr}}{M_{1min}}} = 1, \quad (5.2)$$

where  $D_{max}$  is the maximum value of duty cycle required by the power stage,  $M_{1min}$  is the on-slope of the inductor current corresponding to the duty cycle  $D_{max}$ , and  $M_{3cr}$  is the critical value of compensation slope required by the system to be marginally stable at  $D_{max}$ . Rearranging (5.2), we get

$$1 + \frac{M_{3cr}}{M_{1min}} = \frac{D_{max}}{1 - D_{max}} - \frac{M_{3cr}}{M_{1min}}, \quad (5.3)$$

which gives

$$2 \frac{M_{3cr}}{M_{1min}} = \frac{D_{max}}{1 - D_{max}} - 1. \quad (5.4)$$

Thus,

$$\frac{M_{3cr}}{M_{1min}} = \frac{D_{max} - 0.5}{1 - D_{max}}, \quad (5.5)$$

which results in

$$M_{3cr} = M_{1min} \frac{D_{max} - 0.5}{1 - D_{max}}, \quad (5.6)$$

where  $M_{1min} = fn(D_{max})$  is dependent on converter topology.

### 5.1.1 Buck and Buck-Boost Converters

Using (4.12) and (4.22), the on-slope of the inductor current corresponding to  $D_{max}$  for buck and buck-boost converters is obtained as

$$M_{1min} = M_1 \Big|_{D_{max}} = \frac{V_O}{L} \frac{1 - D_{max}}{D_{max}}. \quad (5.7)$$

Substituting (5.7) into (5.6), the critical value of compensation slope required to ensure marginal stability at  $D_{max}$  is obtained as

$$M_{3cr} = \frac{V_O}{L} \frac{1 - D_{max}}{D_{max}} \frac{D_{max} - 0.5}{1 - D_{max}}, \quad (5.8)$$

which results in

$$M_{3cr} = \frac{V_O}{L} \frac{D_{max} - 0.5}{D_{max}}. \quad (5.9)$$

Therefore, the critical value of required compensation slope normalized with respect to  $V_O/L$  for a given value of  $D_{max}$  is

$$\frac{M_{3cr}}{V_O/L} = \frac{D_{max} - 0.5}{D_{max}}. \quad (5.10)$$

Rearranging (5.9), the limiting value of the duty cycle that can be obtained with a given value of normalized compensation can be obtained as

$$D_{lim} = \frac{0.5}{1 - \frac{M_3}{V_O/L}}. \quad (5.11)$$

Fig. 5.1(a) illustrates the required normalized critical compensation slope as a function of maximum duty cycle for buck and buck-boost converters. The required compensation slope increases in a non-linear fashion as the maximum operating duty cycle increases. The limiting value of duty cycle that can be obtained by a certain value of compensation slope as a function of normalized compensation slope is shown in Fig. 5.1(b).

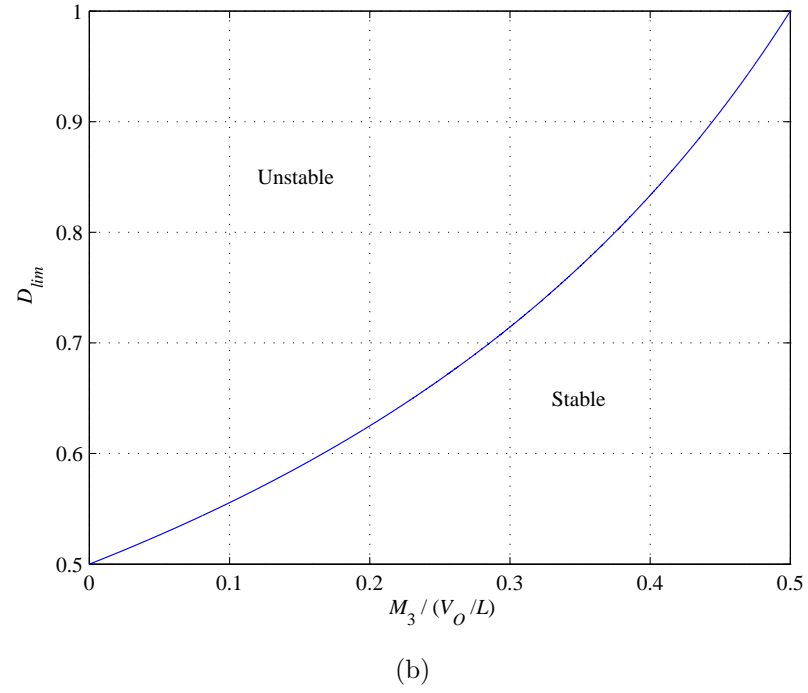
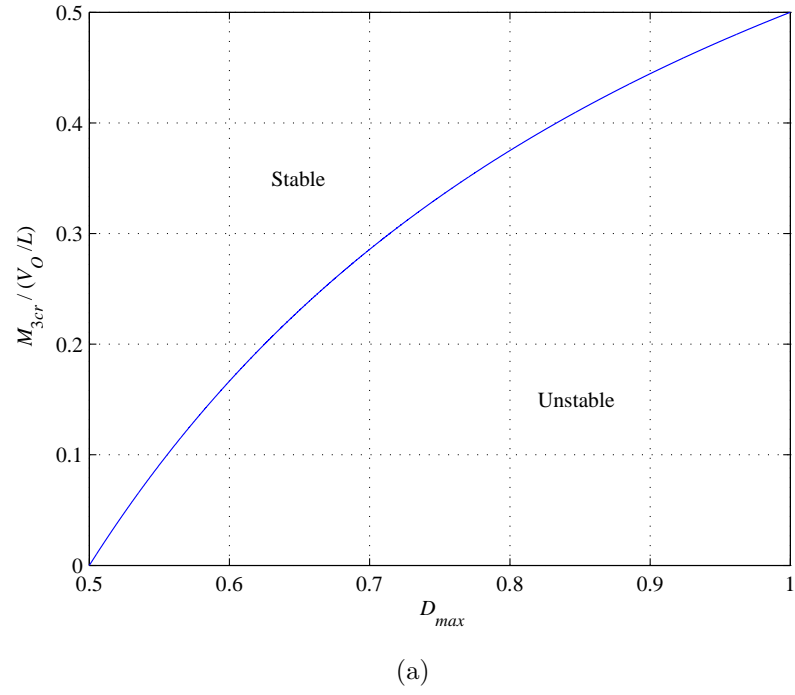


Figure 5.1: Boundary between stable and unstable regions of operations for buck and buck-boost converters. (a)  $M_{3cr}/(V_O/L)$  versus  $D_{max}$ . (b)  $D_{lim}$  versus  $M_3/(V_O/L)$ .

### 5.1.2 Boost Converter

Using (4.17), the minimum on-slope of the inductor current for boost converter is

$$M_{1min} = M_1 \Big|_{D_{max}} = \frac{V_O}{L}(1 - D_{max}). \quad (5.12)$$

Substituting (5.12) into (5.6), the critical compensation slope required for the specified maximum duty cycle  $D_{max}$  is obtained as

$$M_{3cr} = \frac{V_O}{L}(D_{max} - 0.5), \quad (5.13)$$

yielding the required normalized compensation slope as

$$\frac{M_{3cr}}{V_O/L} = D_{max} - 0.5. \quad (5.14)$$

By rearranging (5.14), the limiting value of operating duty cycle as a function of normalized slope compensation can be obtained as

$$D_{lim} = 0.5 + \frac{M_3}{V_O/L}. \quad (5.15)$$

Fig. 5.2(a) shows that the value of required compensation slope increases linearly as the maximum operating duty cycle increases. The linear variation of the limiting duty cycle with the variation in compensation slope is shown in Fig. 5.2(b).

## 5.2 Relative Stability

Using (5.1), the minimum required compensation slope  $M_{3min}$  for a specified value of  $D_{max}$  can be obtained as follows. Rearranging (5.1), we get

$$a \left( 1 + \frac{M_{3min}}{M_{1min}} \right) = \frac{D_{max}}{1 - D_{max}} - \frac{M_{3min}}{M_{1min}} \quad (5.16)$$

and

$$a + (1 + a) \frac{M_{3min}}{M_{1min}} = \frac{D_{max}}{1 - D_{max}}, \quad (5.17)$$

which gives

$$\frac{M_{3min}}{M_{1min}} = \frac{(1 - a)D_{max} - a}{(1 - D_{max})(1 + a)}. \quad (5.18)$$

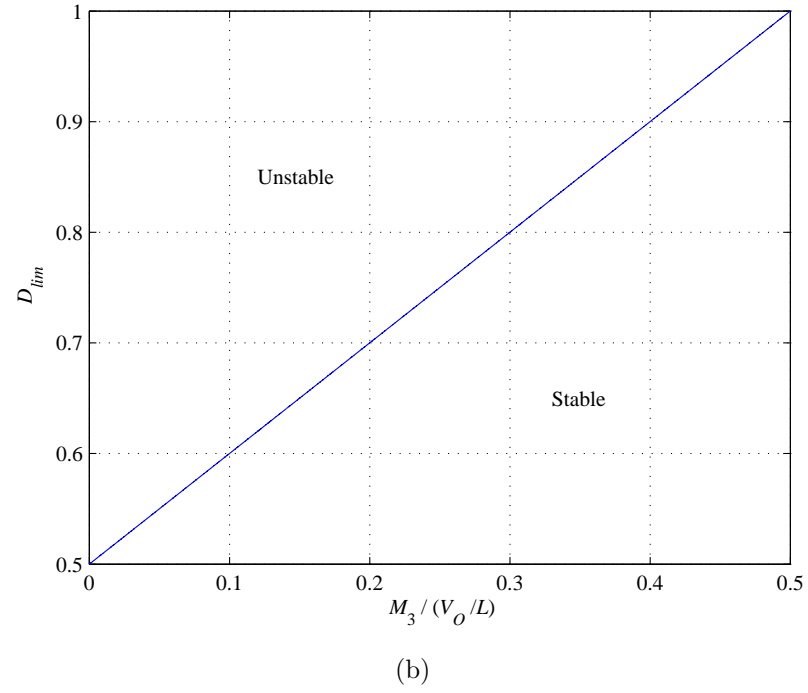
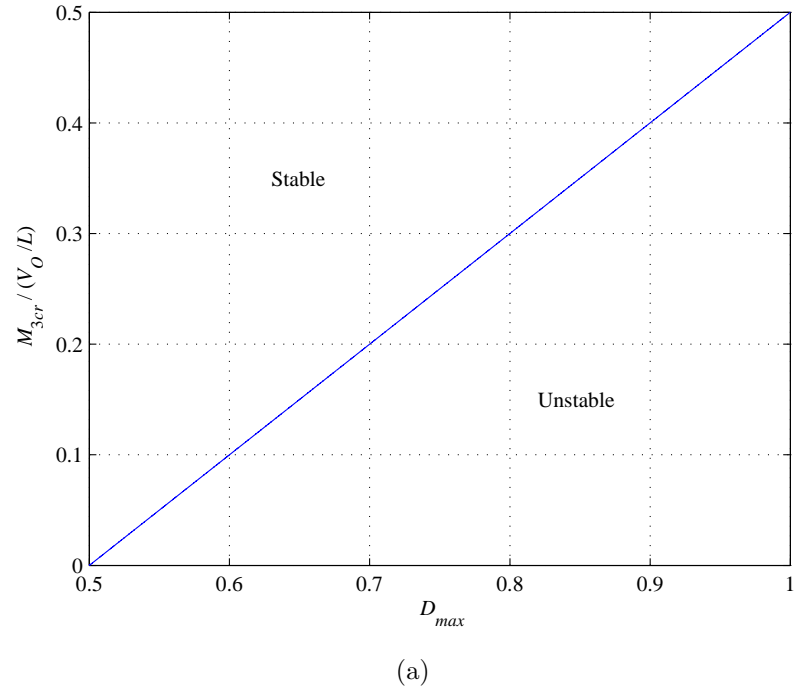


Figure 5.2: Boundary between stable and unstable regions of operations for boost converter. (a)  $M_{3cr}/(V_O/L)$  versus  $D_{max}$ . (b)  $D_{lim}$  versus  $M_3/(V_O/L)$ .

Therefore,

$$\frac{M_{3min}}{M_{1min}} = \frac{D_{max} - \frac{a}{1+a}}{1 - D_{max}}. \quad (5.19)$$

Using (3.27),

$$\frac{a}{1+a} = 0.5 - \frac{\tan PM}{\pi \sqrt[4]{1 + \tan^2 PM}}. \quad (5.20)$$

Substituting (5.20) into (5.19), we get

$$\begin{aligned} \frac{M_{3min}}{M_{1min}} &= \frac{D_{max} - 0.5 + \frac{\tan PM}{\pi \sqrt[4]{1 + \tan^2 PM}}}{1 - D_{max}} \\ &= \frac{D_{max} - 0.5}{1 - D_{max}} + \frac{\tan PM}{\pi(1 - D_{max}) \sqrt[4]{1 + \tan^2 PM}}. \end{aligned} \quad (5.21)$$

Therefore, the minimum value of compensation slope  $M_{3min}$  required at a given value of  $D_{max}$  and at a specified phase margin  $PM$  is

$$\begin{aligned} M_{3min} &= M_{1min} \frac{D_{max} - 0.5}{1 - D_{max}} + M_{1min} \frac{\tan PM}{\pi(1 - D_{max}) \sqrt[4]{1 + \tan^2 PM}} \\ &= M_{3cr} + M_{3PM}. \end{aligned} \quad (5.22)$$

Equation (5.22) gives a general expression for the required minimum compensation slope as a function of maximum duty cycle and phase margin. As the required phase margin  $PM$  increases, the minimum compensation slope  $M_{3min}$  required to obtain a given value of  $D_{max}$  increases. To ensure that the system operates at a specified margin of stability, the minimum required compensation slope  $M_{3min}$  is greater than the critical value  $M_{3cr}$  required for marginal stability by a factor of  $M_{3PM}$ .

As already mentioned, the minimum on-slope of the inductor current is dependent on converter topology. Specific expressions for  $M_{3min}$  for buck, boost, and buck-boost converters will be derived in the following sections.

### 5.2.1 Buck and Buck-Boost Converters

Substituting (5.7) in (5.22), the required amount of minimum slope compensation  $M_{3min}$  as a function of  $D_{max}$  and  $PM$  can be obtained as

$$M_{3min} = \frac{V_O}{L} \frac{D_{max} - 0.5}{D_{max}} + \frac{V_O}{L} \frac{\tan PM}{\pi D_{max} \sqrt[4]{1 + \tan^2 PM}}$$

$$= M_{3cr} + M_{3PM}. \quad (5.23)$$

The required minimum value of compensation slope normalized with respect to  $V_O/L$  at  $D_{max}$  and  $PM$  for buck and buck-boost converters is

$$\begin{aligned} \frac{M_{3min}}{V_O/L} &= \frac{D_{max} - 0.5}{D_{max}} + \frac{\tan PM}{\pi D_{max} \sqrt[4]{1 + \tan^2 PM}} \\ &= \frac{M_{3cr}}{V_O/L} + \frac{M_{3PM}}{V_O/L}. \end{aligned} \quad (5.24)$$

Fig. 5.3(a) illustrates the variation of minimum slope compensation required as a function of  $D_{max}$  at specified values of  $PM$ . When  $PM = 0^\circ$ ,  $M_{3min}$  reduces to  $M_{3cr}$ . As  $PM$  increases, the required slope compensation increases to obtain a given value of  $D_{max}$ . For example, to obtain a maximum duty cycle  $D_{max} = 0.8$ , the required normalized compensation slope increases from 0.375 to 0.8623 as the  $PM$  increases from  $0^\circ$  to  $60^\circ$ .

Multiplying both sides of (5.24) by  $D_{max}$ , we get

$$D_{max} \frac{M_3}{V_O/L} = D_{max} - 0.5 + \frac{\tan PM}{\pi \sqrt[4]{1 + \tan^2 PM}} \quad (5.25)$$

and

$$D_{max} \left( 1 - \frac{M_3}{V_O/L} \right) = 0.5 - \frac{\tan PM}{\pi \sqrt[4]{1 + \tan^2 PM}}, \quad (5.26)$$

which results in

$$D_{max} = \frac{0.5}{1 - \frac{M_3}{V_O/L}} - \frac{\tan PM}{\pi \left( 1 - \frac{M_3}{V_O/L} \right) \sqrt[4]{1 + \tan^2 PM}} \quad (5.27)$$

The maximum duty cycle that can be obtained as a function of normalized minimum compensation slope at given values values of phase margin is depicted in Fig. 5.3(b). When  $PM = 0^\circ$ ,  $D_{max} = D_{lim}$ . As the required phase margin  $PM$  increases, the maximum duty cycle at a given value of compensation slope decreases. Without slope compensation, i.e.,  $M_3 = 0$ , as  $PM$  increases from  $0^\circ$  to  $60^\circ$ , the maximum duty cycle decreases from 0.5 to 0.1102.

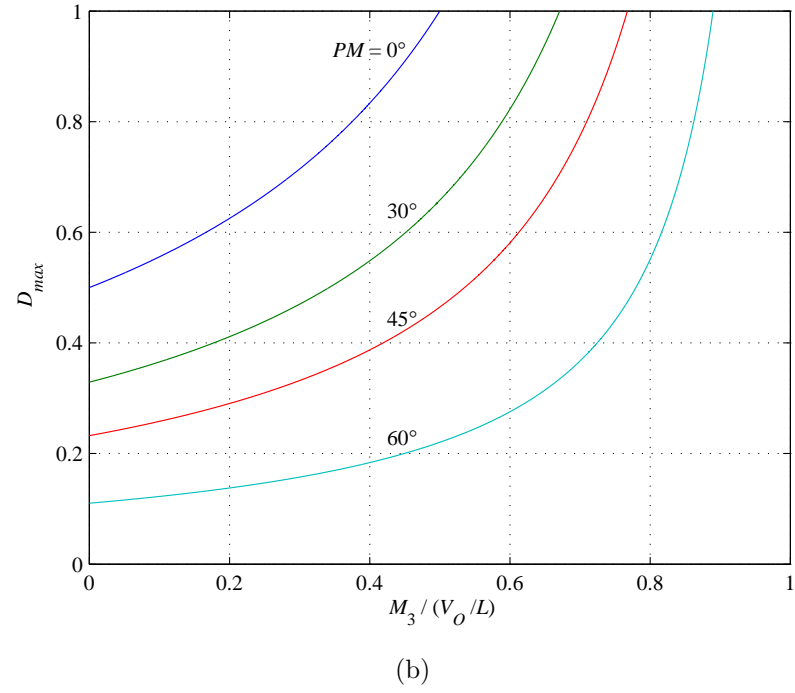
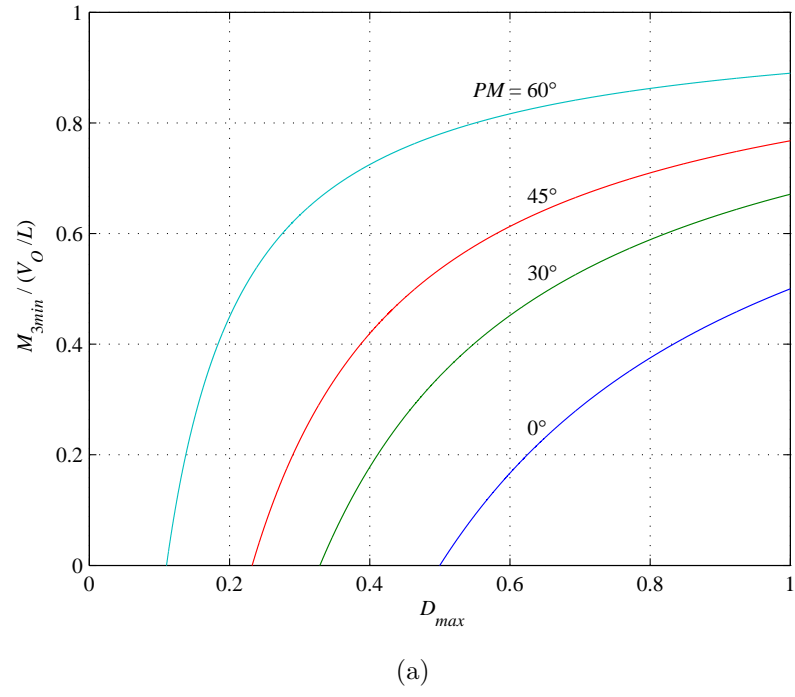


Figure 5.3: Minimum value of required compensation slope to achieve a specified phase margin for buck and buck-boost converters. (a)  $M_{3min}/(V_O/L)$  versus  $D_{max}$ . (b)  $D_{max}$  versus  $M_3/(V_O/L)$ .



### 5.2.2 Boost Converter

Substituting (5.12) into (5.22), the minimum value of slope compensation required to obtain a given value of  $D_{max}$  and  $PM$  is obtained as

$$\begin{aligned} M_{3min} &= \frac{V_O}{L}(D_{max} - 0.5) + \frac{V_O}{L} \frac{\tan PM}{\pi \sqrt[4]{1 + \tan^2 PM}} \\ &= M_{3cr} + M_{3PM}. \end{aligned} \quad (5.28)$$

Therefore, the required normalized slope compensation as a function of maximum duty cycle and phase margin for boost converter is

$$\begin{aligned} \frac{M_{3min}}{V_O/L} &= D_{max} - 0.5 + \frac{\tan PM}{\pi \sqrt[4]{1 + \tan^2 PM}} \\ &= \frac{M_{3cr}}{V_O/L} + \frac{M_{3PM}}{V_O/L}. \end{aligned} \quad (5.29)$$

Also, rearranging (5.29) yielded an expression for the maximum duty cycle as a function of normalized slope compensation and phase margin as shown below.

$$D_{max} = 0.5 + \frac{M_3}{V_O/L} - \frac{\tan PM}{\pi \sqrt[4]{1 + \tan^2 PM}}. \quad (5.30)$$

Fig. 5.4(a) and (b) illustrates (5.29) and (5.30) at selected values of  $PM$ , respectively. As seen from Fig. 5.4(a), the required normalized compensation slope to obtain a given maximum duty cycle increases as the phase margin increases. When  $PM = 0^\circ$ ,  $M_{3min} = M_{3cr}$ . Fig. 5.4(b) shows that the maximum duty cycle that can be obtained by a given amount of slope compensation decreases as the margin of stability of increases.

### 5.3 General Equation for Control Current Level with Slope Compensation

Fig. 5.5 shows the steady-state inductor current  $i_L$  waveform with control current  $I_{CS}$  with slope compensation. Using the geometry, the dc level of control current required

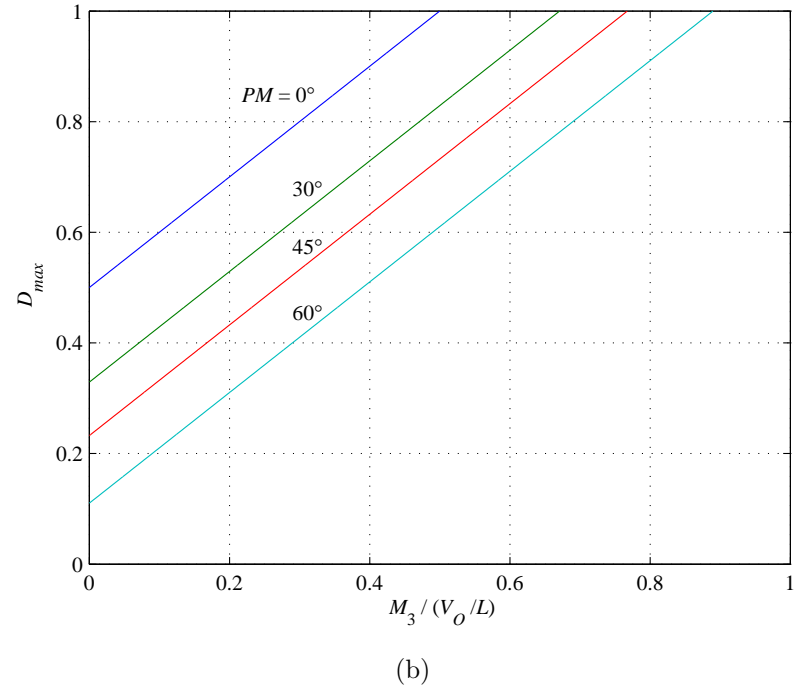
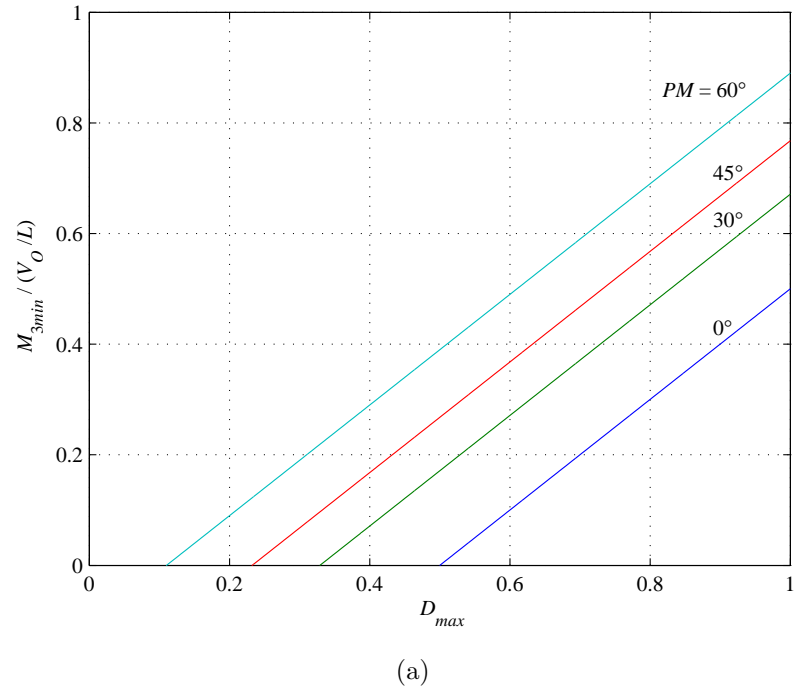


Figure 5.4: Minimum value of required compensation slope to achieve a specified phase margin for boost converter. (a)  $M_{3min}/(V_O/L)$  versus  $D_{max}$ . (b)  $D_{max}$  versus  $M_3/(V_O/L)$ .

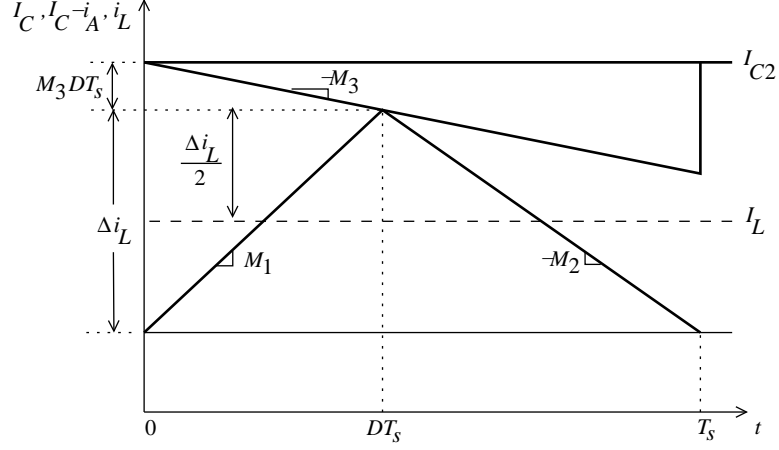


Figure 5.5: Steady-state inductor current  $i_L$  waveform and control current  $I_{CS}$  with slope compensation.

by the inner-current loop with slope compensation is obtained as

$$I_{CS} = I_L + \frac{\Delta i_L}{2} + M_3 D T_s = I_L + \frac{M_1 D}{2 f_s} + \frac{M_3 D}{f_s}. \quad (5.31)$$

Therefore, the dc level of the control current required is a function of the average inductor current  $I_L$ , the on-slope of the inductor current  $M_1$ , the compensation slope  $M_3$ , the duty cycle  $D$ , and the switching frequency  $f_s$ . As already mentioned, the values of  $I_L$ ,  $M_1$ , and  $M_3$  are dependent on the converter topologies.

### 5.3.1 Buck Converter

Using (4.11), (4.12), and (5.23), (5.31) can be expanded to obtain the control current level required by peak current-mode controlled buck converter with slope compensation. Therefore, for a buck converter, the required control current is given by

$$I_{CS} = I_O + \frac{D}{2 f_s} \frac{V_O (1 - D)}{D L} + \frac{D}{f_s} \frac{V_O}{L} \left[ \frac{D_{max} - 0.5}{D_{max}} + \frac{\tan PM}{\pi D_{max} \sqrt[4]{1 + \tan^2 PM}} \right], \quad (5.32)$$

which reduces to

$$I_{CS} = I_O + \frac{V_O}{f_s L} \left[ \frac{1 - D}{2} + D \left( \frac{D_{max} - 0.5}{D_{max}} + \frac{\tan PM}{\pi D_{max} \sqrt[4]{1 + \tan^2 PM}} \right) \right]. \quad (5.33)$$

### 5.3.2 Boost Converter

The control current level for a peak current-mode controlled boost converter with slope compensation can be derived by substituting (4.16), (4.17), and (5.28) into (5.31). Therefore, for a boost converter,

$$I_{CS} = \frac{I_O}{1-D} + \frac{D}{2f_s} \frac{V_O(1-D)}{L} + \frac{D}{f_s} \frac{V_O}{L} \left[ D_{max} - 0.5 + \frac{\tan PM}{\pi \sqrt[4]{1 + \tan^2 PM}} \right] \quad (5.34)$$

which results in

$$I_{CS} = \frac{I_O}{1-D} + \frac{V_O D}{f_s L} \left[ \frac{1-D}{2} + D_{max} - 0.5 + \frac{\tan PM}{\pi \sqrt[4]{1 + \tan^2 PM}} \right] \quad (5.35)$$

### 5.3.3 Buck-Boost Converter

Substituting (4.21), (4.22), and (5.23) into (5.31), the control current level for a buck-boost converter with slope compensated peak current-mode control is obtained as

$$I_{CS} = \frac{I_O}{1-D} + \frac{D}{2f_s} \frac{V_O(1-D)}{DL} + \frac{D}{f_s} \frac{V_O}{L} \left[ \frac{D_{max} - 0.5}{D_{max}} + \frac{\tan PM}{\pi D_{max} \sqrt[4]{1 + \tan^2 PM}} \right], \quad (5.36)$$

which simplifies into

$$I_{CS} = \frac{I_O}{1-D} + \frac{V_O}{f_s L} \left[ \frac{1-D}{2} + D \left( \frac{D_{max} - 0.5}{D_{max}} + \frac{\tan PM}{\pi D_{max} \sqrt[4]{1 + \tan^2 PM}} \right) \right]. \quad (5.37)$$

## 5.4 Design Example

The inner-current loop of a peak current-mode controlled PWM dc-dc buck converter will be designed in this section. The converter specifications were:  $16 \leq V_I \leq 28$  V,  $V_O = 12$  V,  $I_O = 1.2$  A,  $L = 254$   $\mu$ H,  $C = 100$   $\mu$ F,  $R_L = 10$   $\Omega$ , and  $f_s = 100$  kHz. The maximum and minimum values of duty cycle for the converter are, respectively

$$D_{max} = \frac{V_O}{V_{Imin}} = \frac{12}{16} = 0.75 \quad (5.38)$$

and

$$D_{min} = \frac{V_O}{V_{I_{max}}} = \frac{12}{28} = 0.4286. \quad (5.39)$$

Therefore, the range of operating duty cycle is  $D = \langle 0.4286, 0.75 \rangle$ . Since,  $D_{max} > 0.5$ , slope compensation is required for a stable operation.

#### 5.4.1 Required Compensation Slope

Using (5.9), the critical value of compensation slope  $M_{3cr}$  required for the inner loop to be stable at  $D_{max} = 0.75$  is

$$M_{3cr} = \frac{V_O}{L} \frac{D_{max} - 0.5}{D_{max}} = \frac{12}{254 \times 10^{-6}} \frac{0.75 - 0.5}{0.75} = 15.748 \text{A/ms}. \quad (5.40)$$

But, for the inner loop to operate at  $D_{max} = 0.75$  with a stability margin of  $PM = 60^\circ$ , the compensation slope  $M_3$  should be greater than  $M_{3cr}$ . As shown in Section 5.2.1, the minimum value of required compensation slope to have a specified value of  $PM$  is

$$M_{3min} = M_{3cr} + M_{3PM}, \quad (5.41)$$

where

$$M_{3PM} = \frac{V_O}{L} \frac{\tan PM}{\pi D_{max} \sqrt[4]{1 + \tan^2 PM}}. \quad (5.42)$$

Therefore, at  $PM = 60^\circ$ ,

$$M_{3PM} = \frac{12}{254 \times 10^{-6}} \frac{\tan 60^\circ}{\pi 0.75 \sqrt[4]{1 + \tan^2 60^\circ}} = 24.557 \text{A/ms}. \quad (5.43)$$

Thus, the total minimum compensation slope required to have a phase margin of  $60^\circ$  at  $D_{max} = 0.75$  is obtained as

$$M_{3min} = M_{3cr} + M_{3PM} = 15.748 + 24.557 = 40.305 \text{A/ms}. \quad (5.44)$$

The amplitude of the compensation ramp with the required minimum slope is

$$I_A = \frac{M_{3min}}{f_s} = \frac{40.305 \times 10^3}{100 \times 10^3} = 0.403 \text{ A}. \quad (5.45)$$

Table 5.1 shows the compensation slope and ramp amplitude required to obtain specified values of  $PM$  at  $D_{max} = 0.75$ .

Table 5.1: Minimum compensation slope  $M_{3min}$  and amplitude of the compensation ramp to obtain  $D_{max} = 0.75$  at given values of  $PM$ .

$PM$ ( $^\circ$ )	$M_{3PM}$ (A/ms)	$M_{3min}$ (A/ms)	$I_A$ (A)
$60^\circ$	24.557	40.305	0.40305
$45^\circ$	16.861	32.609	0.32609
$30^\circ$	10.773	26.521	0.26521
$0^\circ$	0	15.748	0.15748

#### 5.4.2 Required Control Current

The control current required to obtain the whole duty cycle range at each slope compensation given in Table 5.1 can be calculated using (5.33) in Section 5.3.1. The resultant control current values along with duty cycle values and corresponding input voltage values are shown in Table 5.4.1. To have  $PM = 60^\circ$ , the range of control current values required to obtain the required duty cycle range is  $I_{CS} = \langle 1.508, 1.561 \rangle$ . The range of control current required by the inner-current loop has to be known to design the outer-voltage loop, since the outer-voltage loop supplies the control voltage  $V_{CS} = R_s I_{CS}$ . This is also necessary for the proper selection of the sense resistor so that the comparator will not saturate.

### 5.5 Simulation Results

The designed PWM dc-dc buck converter with slope compensation as shown in Fig. 4.6 was simulated using Saber Sketch. A comparison of the theoretical values obtained in Section 5.3.1 and the simulation results is shown in Fig. 5.6. The duty cycle obtained by using the calculated values of  $I_{CS}$  agreed with the values in Table 5.4.1. The control voltage  $V_{CS} = R_s I_{CS}$ , compensating ramp  $v_A$ , sensed inductor current  $R_s i_L$ , and MOSFET gate-to-source voltage  $V_{GS}$  waveforms obtained for  $PM = 60^\circ$  using the values given in Table 5.4.1 are shown in Figs. 5.7-5.8. Figs. 5.9-5.10 show the corresponding waveforms at  $PM = 45^\circ$ . Waveforms for  $PM = 30^\circ$  and  $0^\circ$  are

Table 5.2: Minimum compensation slope  $M_{3min}$  and control current to obtain  $D_{max} = 0.75$  at given values of  $PM$  and duty cycle  $D$ .

$PM$ ( $^\circ$ )	$M_{3min}$ (A/ms)	$D$	$V_I$ (V)	$I_{CS}$ (A)
$60^\circ$	40.305	0.43	28	1.508
		0.45	26.67	1.511
		0.5	24	1.52
		0.55	21.82	1.528
		0.6	20	1.536
		0.65	18.46	1.545
		0.7	17.14	1.553
		0.75	16	1.561
$45^\circ$	32.609	0.43	28	1.475
		0.45	26.67	1.477
		0.5	24	1.481
		0.55	21.82	1.486
		0.6	20	1.49
		0.65	18.46	1.495
		0.7	17.14	1.499
		0.75	16	1.504
$30^\circ$	26.521	0.43	28	1.449
		0.45	26.67	1.449
		0.5	24	1.451
		0.55	21.82	1.452
		0.6	20	1.454
		0.65	18.46	1.455
		0.7	17.14	1.457
		0.75	16	1.458
$0^\circ$	15.748	0.43	28	1.402
		0.45	26.67	1.401
		0.5	24	1.397
		0.55	21.82	1.393
		0.6	20	1.389
		0.65	18.46	1.385
		0.7	17.14	1.381
		0.75	16	1.377

shown in Figs. 5.11-5.12 and Figs. 5.13-5.14, respectively.

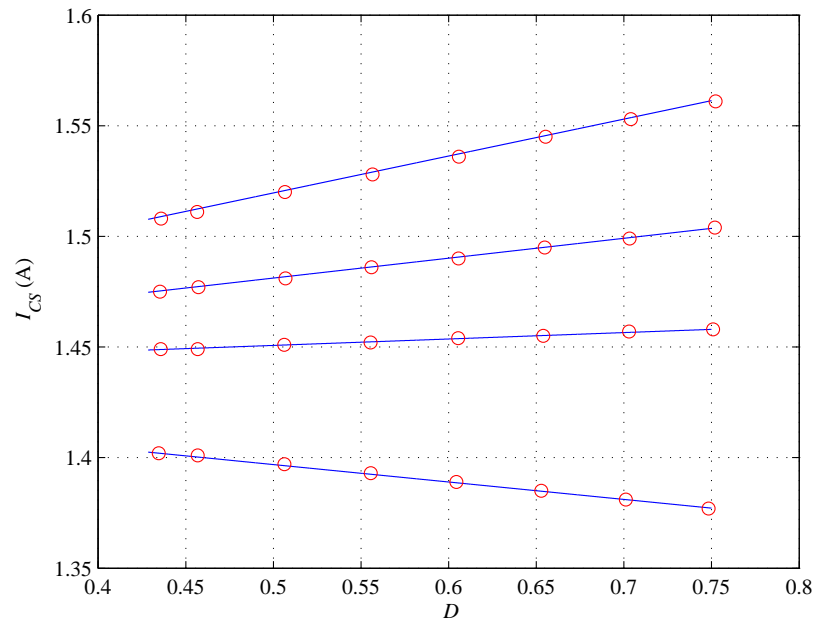
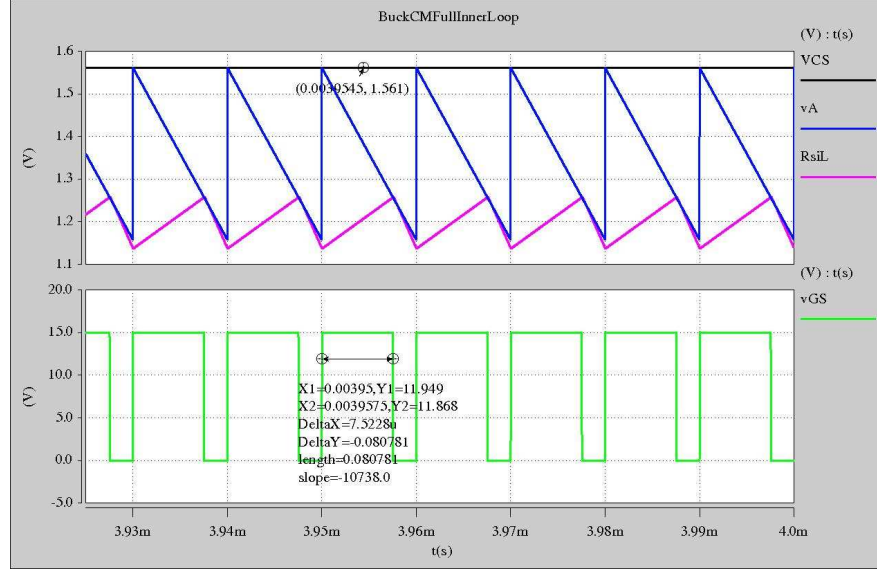
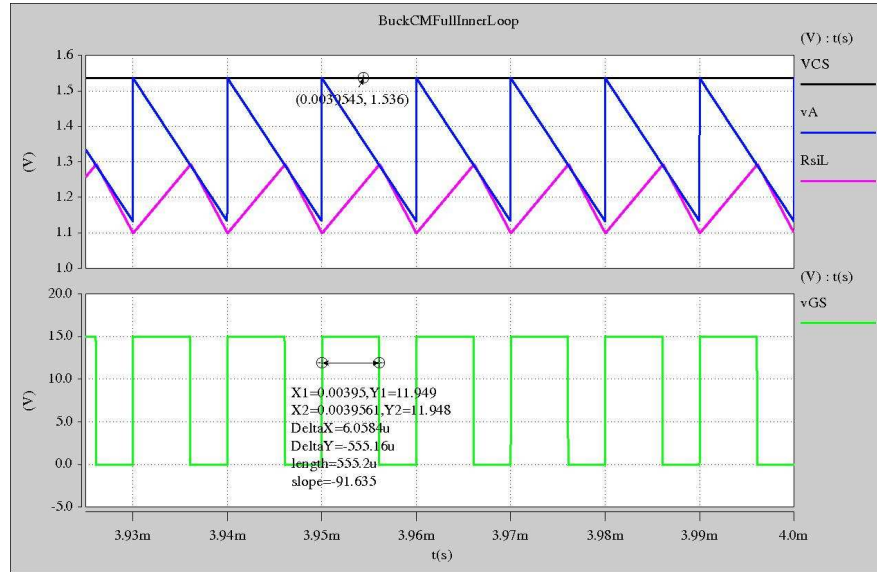


Figure 5.6: Comparison of theoretical and Saber simulation results.



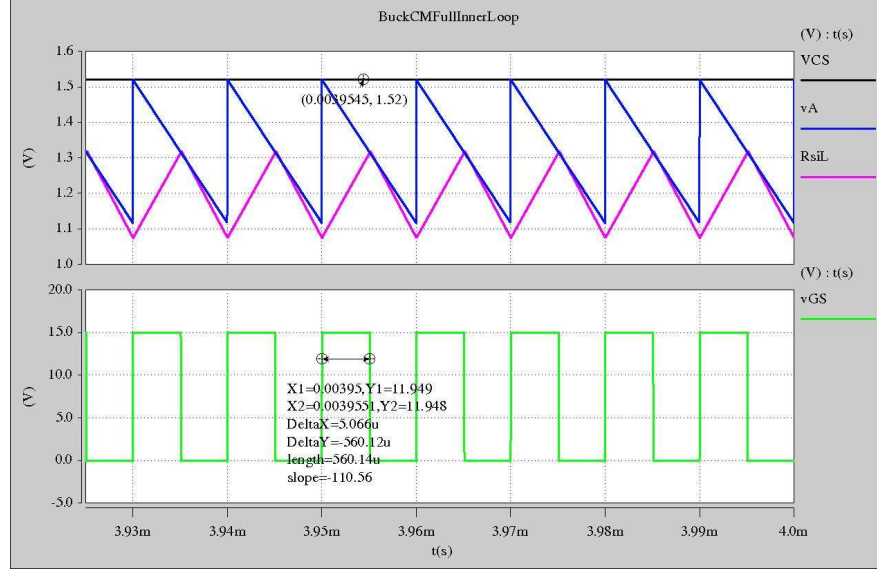


(a)

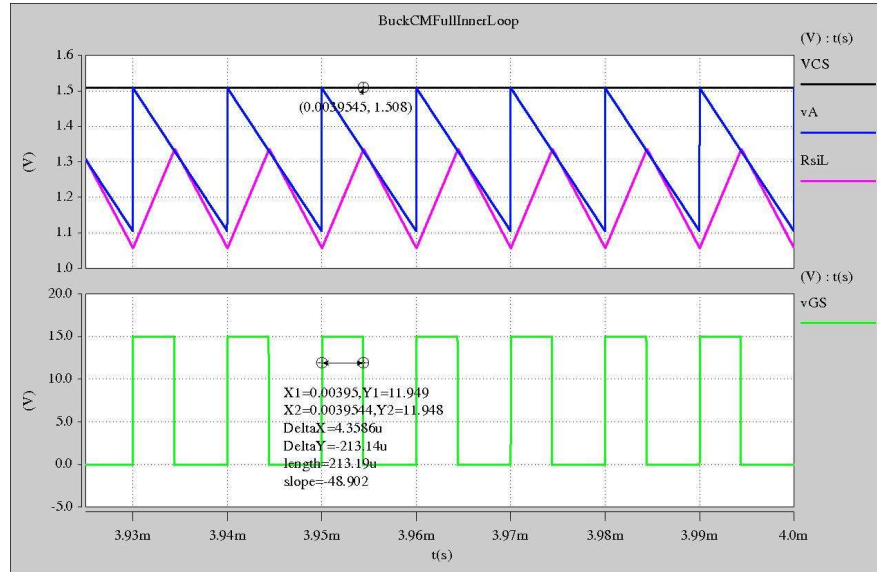


(b)

Figure 5.7: Control voltage  $V_{CS}$ , compensating ramp  $v_A$ , sensed inductor current  $R_s i_L$ , and MOSFET gate-to-source voltage  $V_{GS}$  waveforms obtained using Saber simulations at  $PM = 60^\circ$ . (a)  $V_I = 16$  V and  $V_{CS} = R_s I_{CS} = 1.561$  V. (b)  $V_I = 20$  V and  $V_{CS} = R_s I_{CS} = 1.536$  V.

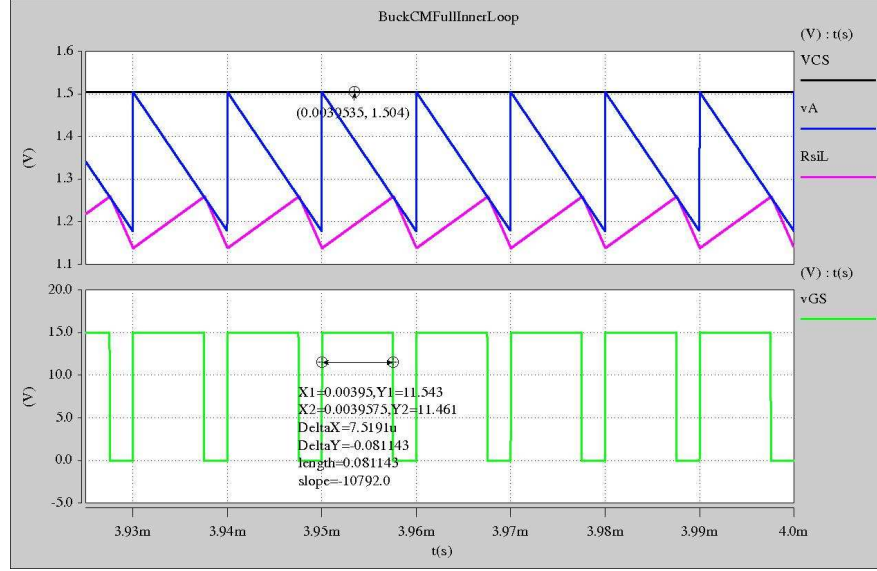


(a)

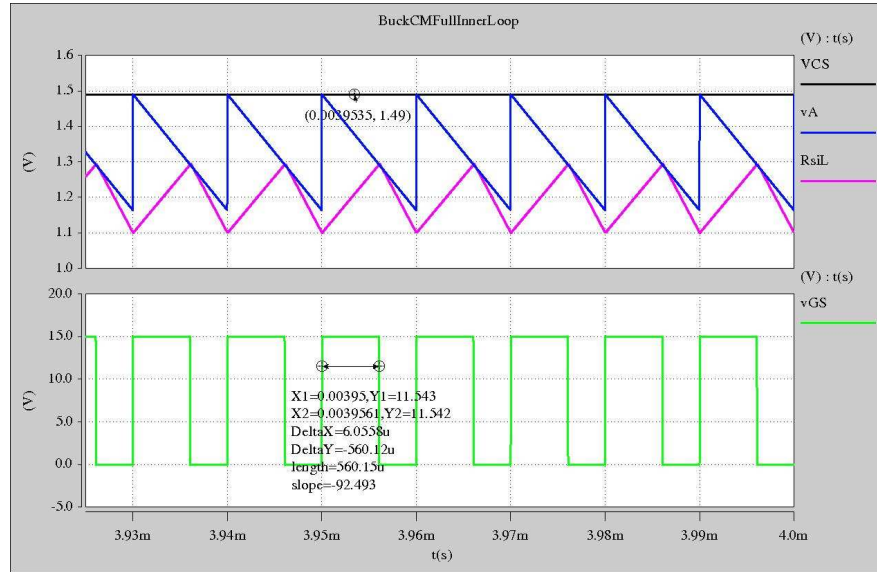


(b)

Figure 5.8: Control voltage  $V_{CS}$ , compensating ramp  $v_A$ , sensed inductor current  $R_s i_L$ , and MOSFET gate-to-source voltage  $V_{GS}$  waveforms obtained using Saber simulations at  $PM = 60^\circ$ . (a)  $V_I = 24$  V and  $V_{CS} = R_s I_{CS} = 1.52$  V. (b)  $V_I = 28$  V and  $V_{CN} = R_s I_{CS} = 1.508$  V.

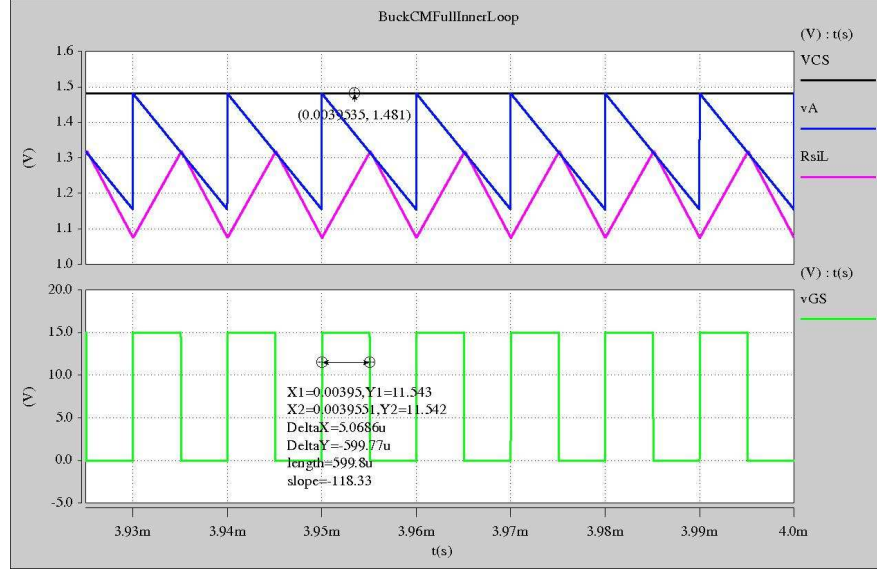


(a)

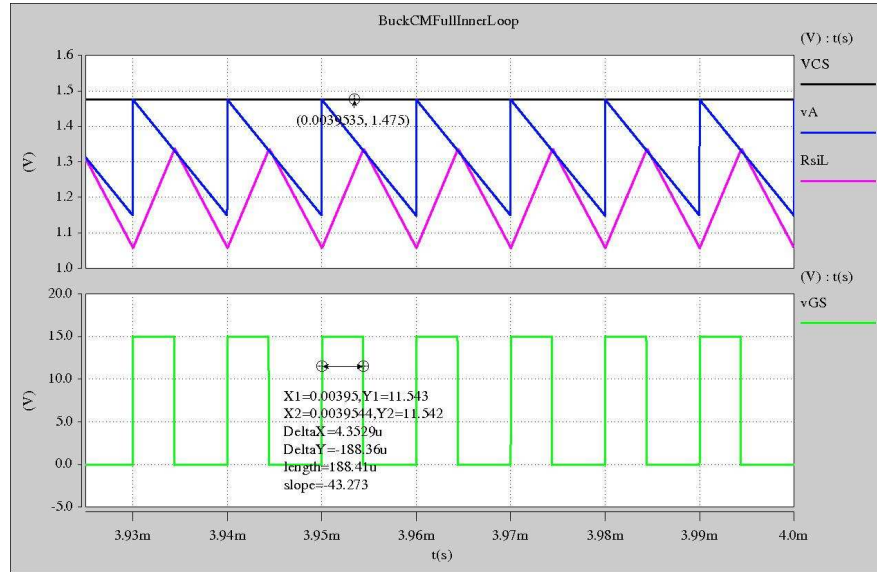


(b)

Figure 5.9: Control voltage  $V_{CS}$ , compensating ramp  $v_A$ , sensed inductor current  $R_s i_L$ , and MOSFET gate-to-source voltage  $V_{GS}$  waveforms obtained using Saber simulations at  $PM = 45^\circ$ . (a)  $V_I = 16$  V and  $V_{CS} = R_s I_{CS} = 1.504$  V. (b)  $V_I = 20$  V and  $V_{CS} = R_s I_{CS} = 1.549$  V.

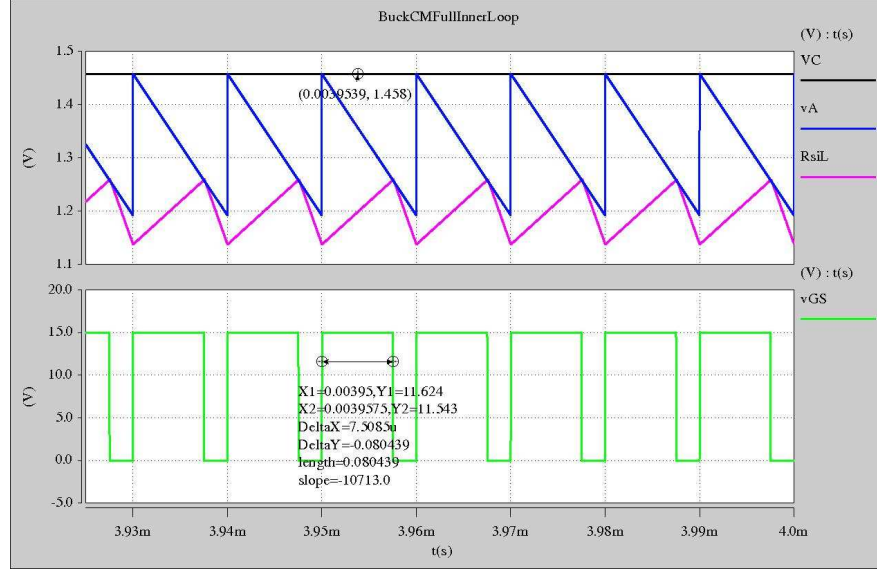


(a)

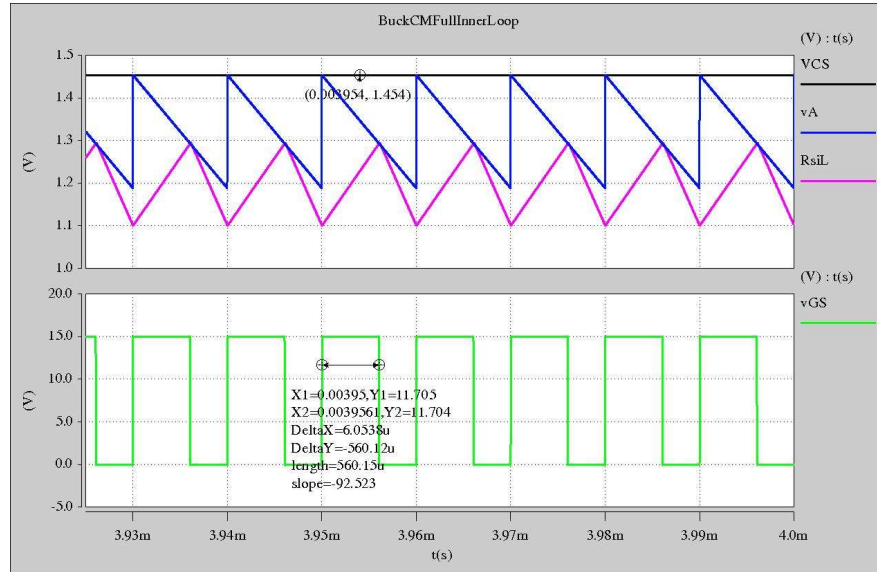


(b)

Figure 5.10: Control voltage  $V_{CS}$ , compensating ramp  $v_A$ , sensed inductor current  $R_s i_L$ , and MOSFET gate-to-source voltage  $V_{GS}$  waveforms obtained using Saber simulations at  $PM = 45^\circ$ . (a)  $V_I = 24$  V and  $V_{CS} = R_s I_{CS} = 1.481$  V. (b)  $V_I = 28$  V and  $V_{CN} = R_s I_{CS} = 1.475$  V.

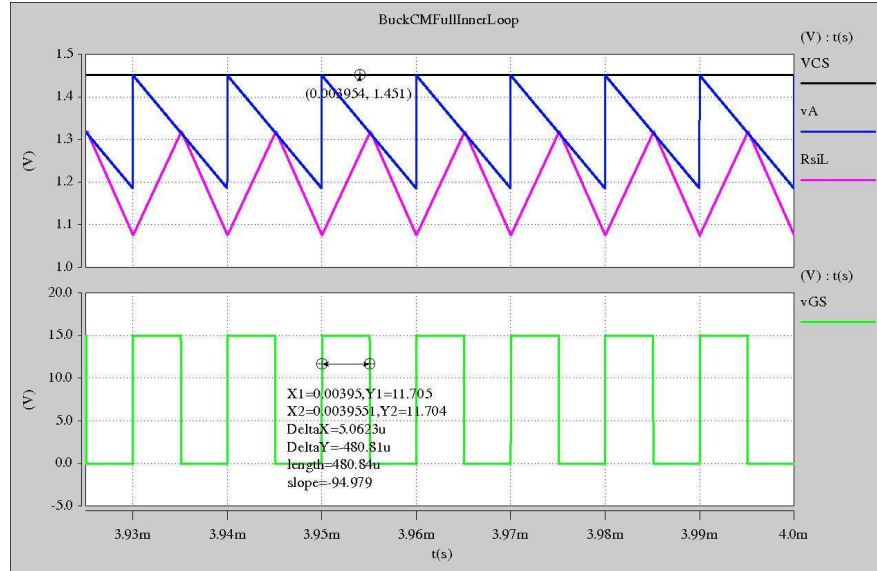


(a)

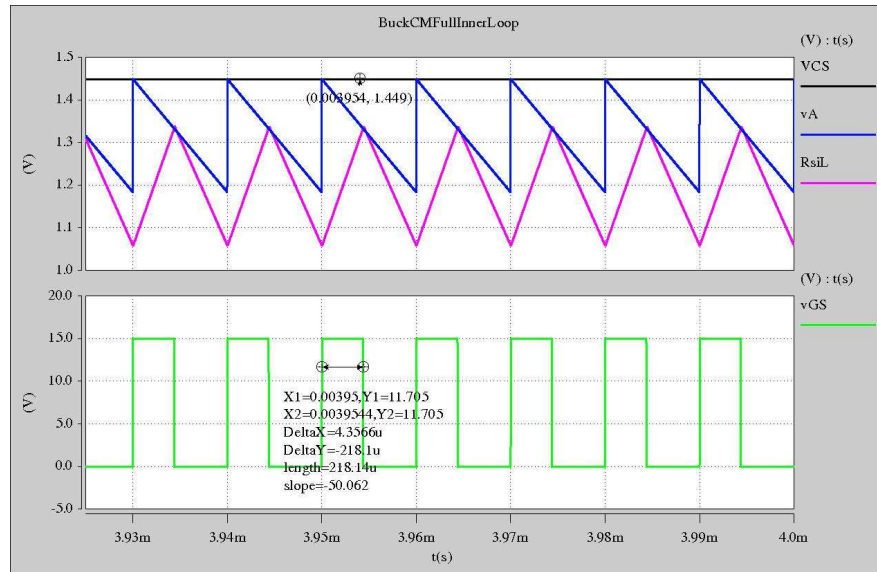


(b)

Figure 5.11: Control voltage  $V_{CS}$ , compensating ramp  $v_A$ , sensed inductor current  $R_s i_L$ , and MOSFET gate-to-source voltage  $V_{GS}$  waveforms obtained using Saber simulations at  $PM = 30^\circ$ . (a)  $V_I = 16$  V and  $V_{CS} = R_s I_{CS} = 1.458$  V. (b)  $V_I = 20$  V and  $V_{CN} = R_s I_{CS} = 1.454$  V.

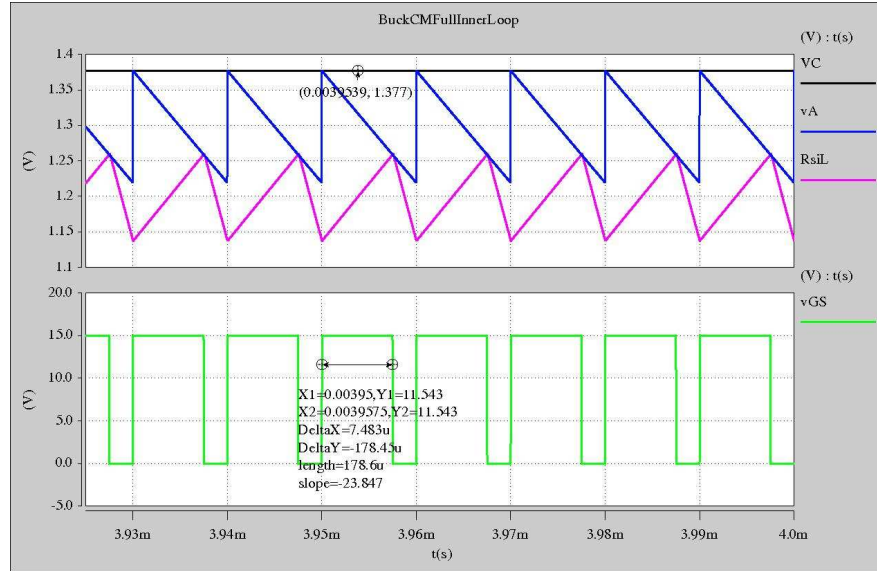


(a)

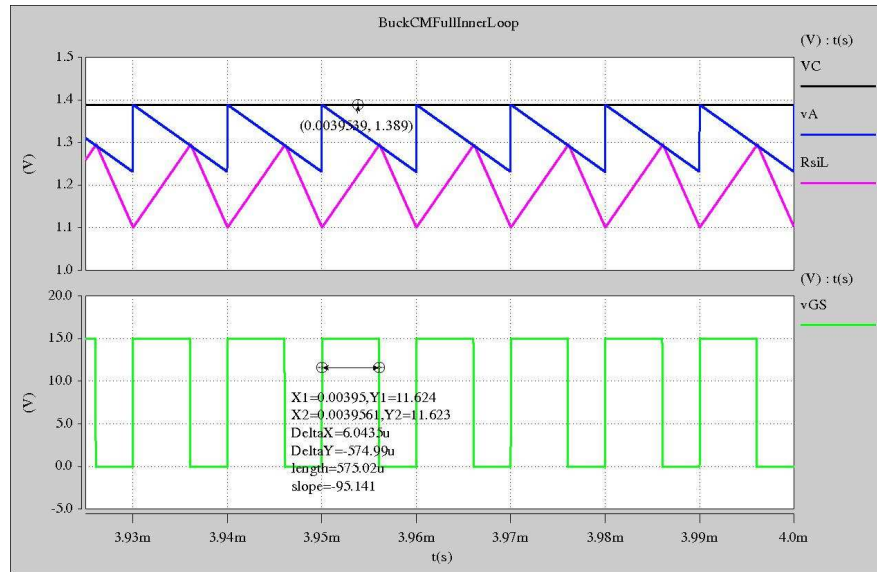


(b)

Figure 5.12: Control voltage  $V_{CS}$ , compensating ramp  $v_A$ , sensed inductor current  $R_s i_L$ , and MOSFET gate-to-source voltage  $V_{GS}$  waveforms obtained using Saber simulations at  $PM = 30^\circ$ . (a)  $V_I = 24$  V and  $V_{CS} = R_s I_{CS} = 1.451$  V. (b)  $V_I = 28$  V and  $V_{CN} = R_s I_{CS} = 1.449$  V.



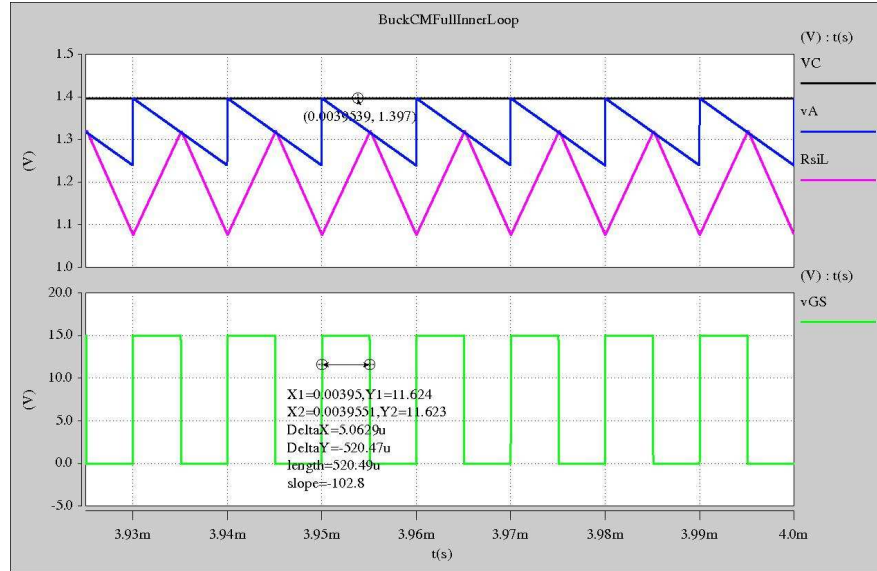
(a)



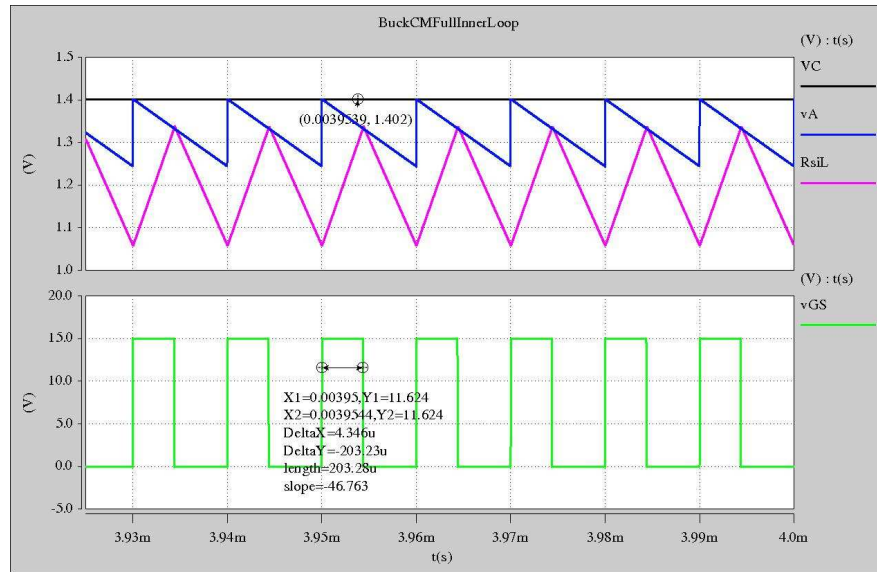
(b)

Figure 5.13: Control voltage  $V_{CS}$ , compensating ramp  $v_A$ , sensed inductor current  $R_s i_L$ , and MOSFET gate-to-source voltage  $V_{GS}$  waveforms obtained using Saber simulations at  $PM = 0^\circ$ . (a)  $V_I = 16$  V and  $V_{CS} = R_s I_{CS} = 1.377$  V. (b)  $V_I = 20$  V and  $V_{CN} = R_s I_{CS} = 1.389$  V.





(a)



(b)

Figure 5.14: Control voltage  $V_{CS}$ , compensating ramp  $v_A$ , sensed inductor current  $R_s i_L$ , and MOSFET gate-to-source voltage  $V_{GS}$  waveforms obtained using Saber simulations at  $PM = 0^\circ$ . (a)  $V_I = 24$  V and  $V_{CS} = R_s I_{CS} = 1.397$  V. (b)  $V_I = 28$  V and  $V_{CN} = R_s I_{CS} = 1.402$  V.



## 6 Dynamic Behavior of the Inner-Current Loop of Peak Current-Mode Controlled PWM DC-DC Buck Converter

In this chapter, the buck converter power stage transfer functions in the critical path of peak current-mode control will be derived. Also, the dynamic behavior of the inner-current loop of peak current-mode controlled PWM dc-dc buck will be analysed. Finally, the control-to-output transfer function of the inner loop will be derived. This transfer function is necessary for the compensator design in the outer loop as it is plant transfer function for the outer loop.

### 6.1 Small-Signal Model of Buck Converter

An open-loop PWM dc-dc buck converter is shown in Fig. 6.1(a). The circuit components are: switching components  $S_1$  and  $D_1$ , passive components  $L$  and  $C$ , and the load resistance  $R_L$ . Let  $v_I = V_I + v_i$  be the total input voltage,  $v_O = V_O + v_o$  be the total output voltage,  $d_T = D + d$  be the total duty cycle, and  $i_L = I_L + i_l$  be the inductor current, where  $V_I$ ,  $V_O$ ,  $D$ , and  $I_L$  are the dc components and  $v_i$ ,  $v_o$ ,  $d$ , and  $i_l$  are the ac components, respectively. Let  $i_o$  be the small signal component of the load current.

The small-signal model of the PWM dc-dc buck converter [17] using energy conservation approach is shown in Fig. 6.1(b). In the figure,  $r_C$  is the capacitor equivalent series resistance (ESR) and the resistance  $r = Dr_{DS} + (1 - D)R_F + r_L$ , where  $r_{DS}$  is the on-resistance of the MOSFET,  $R_F$  is the diode forward resistance, and  $r_L$  is the inductor ESR. From the figure, it is seen that there are three input quantities that would affect the inductor current in the converter: (a) duty cycle, (b) input voltage, and (c) output current. This section analyzes the dynamic behavior of a dc-dc PWM buck converter operating in CCM in response to perturbations in the duty cycle.

The small-signal model to derive duty cycle-to-inductor current and duty ratio-to-

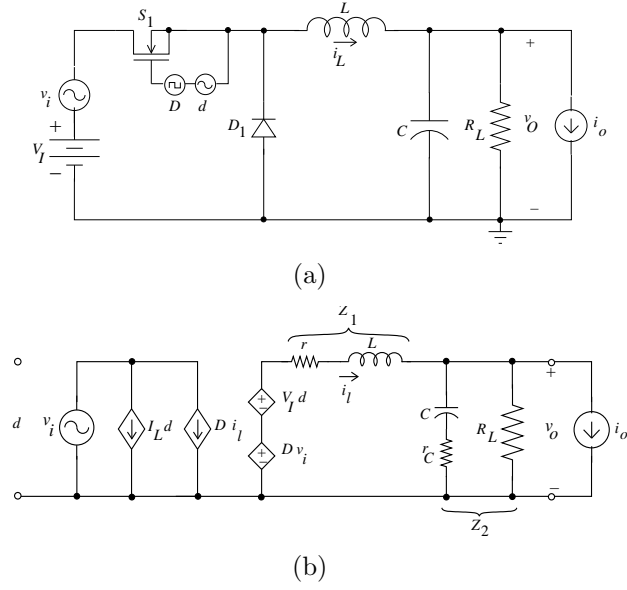


Figure 6.1: Open-loop PWM dc-dc buck converter. (a) Circuit. (b) Small-signal model.

output voltage transfer functions shown in Fig. 6.2(a) is obtained by reducing input voltage and output current to zero in the small signal model of the buck converter shown in Fig. 6.1(b). The small-signal models for wide-frequency (WF), low-frequency (LF), and high-frequency (HF) ranges are shown in Figs. 6.2(a), 6.2(b), and 6.2(c), respectively.

## 6.2 Duty Ratio-to-Inductor Current Transfer Function of Buck Converter

In this section, the duty cycle-to-inductor current transfer function, including parasitics and MOSFET delay, of a buck converter in CCM is derived and illustrated using MatLab simulations. The wide-frequency and high-frequency transfer functions are derived and illustrated using MatLab simulations. The obtained results are verified using experimental results.

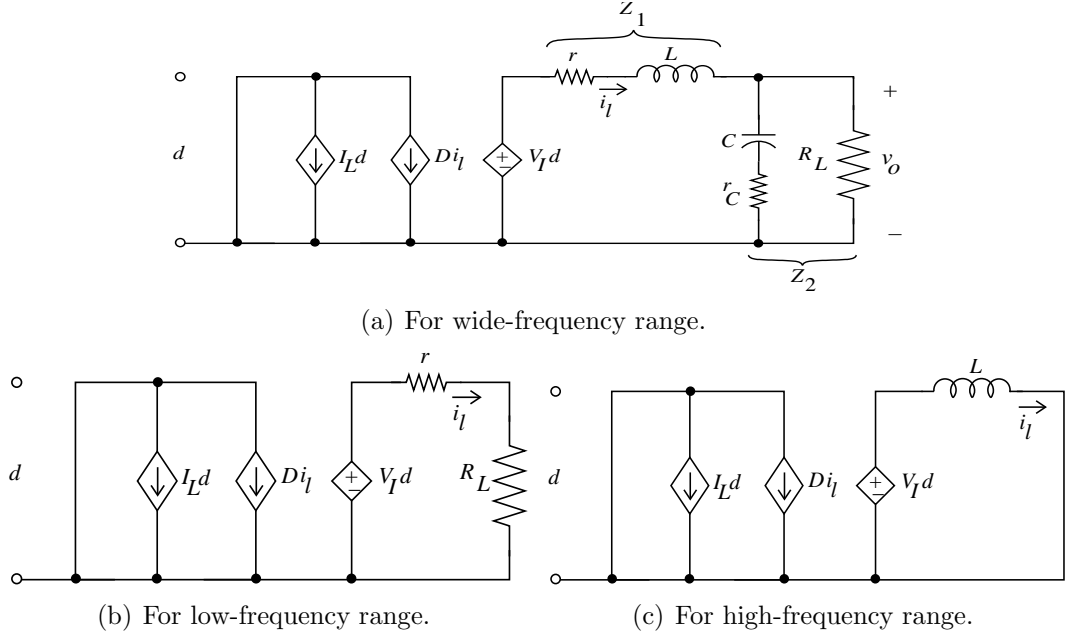


Figure 6.2: Small-signal model of a buck converter to derive duty cycle-to-inductor current and duty cycle-to-output voltage transfer functions.

### 6.2.1 Wide-Frequency Transfer Function

A wide-frequency small-signal model is shown in Fig. 6.2(a). From the figure,

$$i_l(s) = \frac{V_I d(s)}{Z_1(s) + Z_2(s)}, \quad (6.1)$$

where

$$Z_1(s) = r + sL \quad (6.2)$$

and

$$Z_2 = R_L \parallel \left( \frac{1}{sC} + r_C \right) = \frac{R_L(1 + sCr_C)}{1 + sC(R_L + r_C)}. \quad (6.3)$$

Thus, the wide-frequency duty cycle-to-inductor current transfer function is obtained as

$$\begin{aligned} T_{pi}(s) &= \frac{i_l(s)}{d(s)} \Big|_{v_i=i_o=0} = \frac{V_I}{Z_1(s) + Z_2(s)} \\ &= \frac{V_I}{r + sL + \frac{R_L(1+sCr_C)}{1+sC(R_L+r_C)}} = T_{pix} \frac{s + \omega_{zi}}{s^2 + 2\xi\omega_0 s + \omega_0^2}, \end{aligned} \quad (6.4)$$

where

$$T_{pix} = \frac{V_I}{L}, \quad \omega_{zi} = \frac{1}{C(R_L + r_C)}, \quad \omega_0 = \sqrt{\frac{R_L + r}{LC(R_L + r_C)}},$$

$$\text{and } \xi = \frac{C[R_L r_C + r_C r + R_L r] + L}{2\sqrt{LC(R_L + r_C)(R_L + r)}}. \quad (6.5)$$

Including the MOSFET delay [41],

$$T_d(s) = e^{-st_d} \approx -\frac{s - \frac{2}{t_d}}{s + \frac{2}{t_d}}, \quad (6.6)$$

the duty ratio-to-inductor current transfer function becomes

$$T_{pid}(s) = T_{pi}(s)T_d(s) = -T_{pix} \frac{s + \omega_{zi}}{s^2 + 2\xi\omega_0 s + \omega_0^2} \frac{s - \frac{2}{t_d}}{s + \frac{2}{t_d}}. \quad (6.7)$$

### 6.2.2 Low-Frequency Transfer Function

At dc and low frequencies, i.e., for  $0 \leq f \leq f_{zi}$ , the small-signal model of the buck converter in Fig. 6.2(a) reduces to the small-signal model shown in Fig. 6.2(b). Therefore, at low frequencies,  $i_l(s) = \frac{V_I d(s)}{R_L + r}$ . Thus, the duty ratio-to-inductor current transfer function reduces to

$$T_{piLF}(s) = \left. \frac{i_l(s)}{d(s)} \right|_{v_i=i_o=0} = \frac{V_I}{R_L + r}, \quad (6.8)$$

which indicates the power stage is resistive at dc and low frequencies. Also,  $Z_{2LF}(s) = R_L$ .

### 6.2.3 High-Frequency Transfer Function

At high frequencies, i.e., for  $f_0 \leq f \leq f_s/2$ , the small-signal model of the buck converter in Fig. 6.2(a) reduces to the small-signal model shown in Fig. 6.2(c). From Fig. 6.2(c), at high frequencies  $i_l(s) = \frac{V_I d(s)}{sL}$ . Therefore, at high frequencies, the duty cycle-to-inductor current transfer function is

$$T_{piHF}(s) = \left. \frac{i_l(s)}{d(s)} \right|_{v_i=i_o=0} = \frac{V_I}{sL} = T_{pix} \frac{1}{s}, \quad (6.9)$$

which indicates that, the power stage with current-mode control can be modeled as an inductor at high frequencies.

Table 6.1: Corner frequencies and dc gains of  $T_{pi}(s)$  at given values of input voltage.

$V_I$ (V)	$f_{zi}$ (Hz)	$f_0$ (kHz)	$T_{pio}$ (dBA)
16		1.1879	3.841
23.33	222.48	1.1853	7.156
35		1.183	10.707

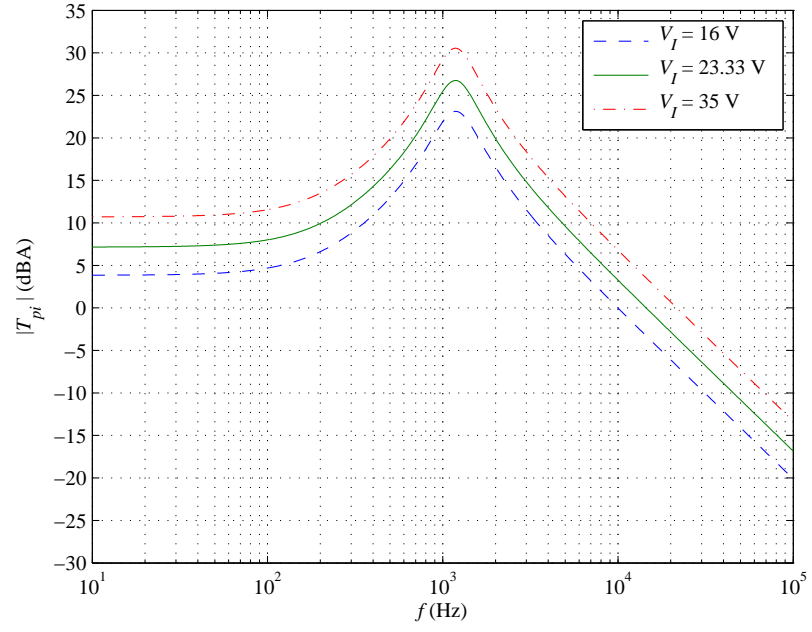
#### 6.2.4 Simulation Results

The selected design had the following parameters:  $V_I = 16 \text{ V} \leq V_I \leq 35 \text{ V}$ ,  $V_O = 7 \text{ V}$ ,  $I_O = 0.7 \text{ A}$ ,  $L = 254 \text{ } \mu\text{H}$ ,  $r_L = 36 \text{ m}\Omega$ ,  $C = 68 \text{ } \mu\text{F}$ ,  $r_C = 520 \text{ m}\Omega$ ,  $R_L = 10 \text{ } \Omega$ ,  $r_{DS} = 0.4 \text{ } \Omega$ ,  $R_F = 0.1 \text{ } \Omega$ ,  $V_F = 0.7 \text{ } \Omega$ , and  $f_s = 100 \text{ kHz}$ . The MOSFET delay is assumed as  $t_d = 0.55 \text{ } \mu\text{s}$ .

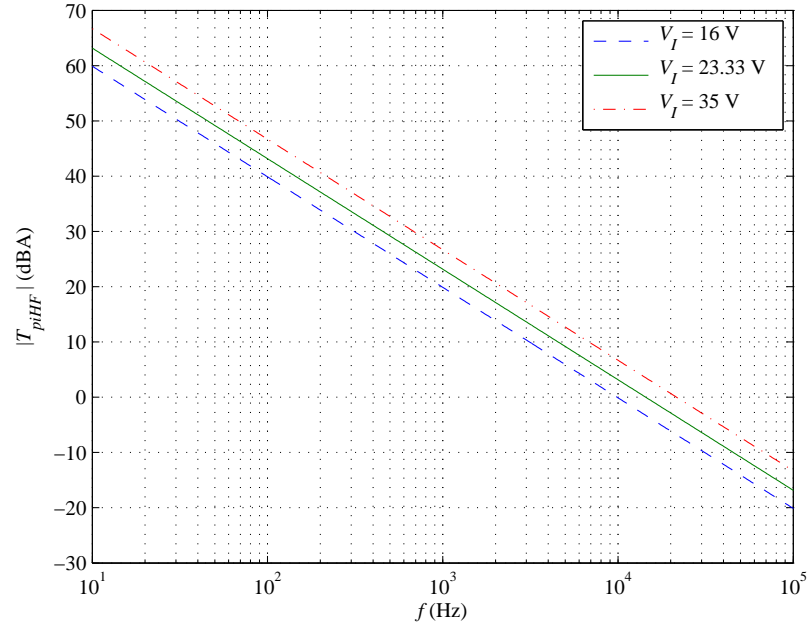
Bode plots illustrating the duty cycle-to-inductor current transfer function at given values of input voltage are shown in Figs. 6.3 and 6.4. The magnitude plots at wide-frequency range and high-frequency range are shown in Fig. 6.3(a) and (b), respectively. Fig. 6.4 depicts a comparison of the phase plots in high-frequency range, wide-frequency range without delay, and wide-frequency range with delay. The wide-frequency transfer function is a low pass filter transfer function with one zero and two complex conjugate poles. The corner frequencies of the zero  $f_{zi}$  as well as the complex poles  $f_0$  and the dc gain  $T_{pio}$  at given values of input voltage is shown in Table 6.1. The high-frequency transfer function is an integrator function. This indicates that the power stage behaves as an inductor at high frequencies. The WF Bode plots without delay converges to the HF Bode plots at high frequencies. As seen from Fig. 6.4, the MOSFET delay component introduces additional phase at high frequencies.

#### 6.2.5 Experimental Results

The buck converter circuit shown in Fig. 6.1(a) was set up with switching components IRF530 power MOSFET and MUR820 power diode. IR2110 was used to drive the high-side MOSFET. The passive component values and the parasitic values were



(a)



(b)

Figure 6.3: Magnitude plots of duty cycle-to-inductor current transfer function at given input voltages. (a) Wide-frequency plots. (b) High-frequency plots.

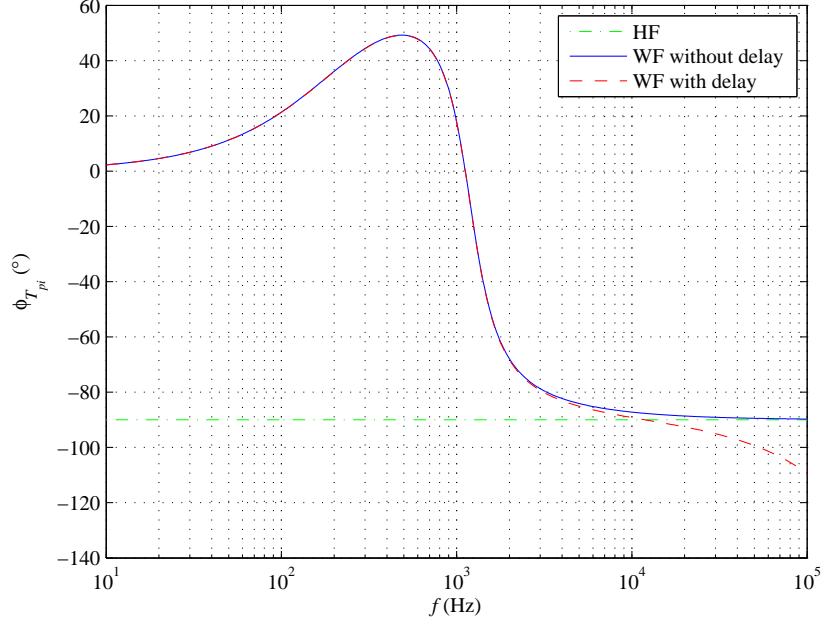


Figure 6.4: Phase plots of duty cycle-to-inductor current transfer function.

measured to be the same as given in section 6.2.4. A duty cycle modulator gain of  $20 \log(1/4) = -12$  dB was introduced by LM357N op-amp used as the comparator with a reference ramp of 4 V. The MOSFET exhibited a delay of  $t_d = 0.55 \mu\text{s}$ . The Bode plots of duty cycle-to-inductor current transfer function were measured using Hewlett-Packard 4194A Impedance/Gain-Phase Analyzer and Pearson model 411 wide-bandwidth current probe. The probe frequency response was measured using a simple resistive load of  $R_L = 1 \Omega$  and the same dc current as in the buck converter design  $I = 0.7$  A. The effect of the probe frequency response on the measured  $T_{pi}$  response was compensated using the compensation function of the 4194A analyzer.

Fig. 6.5 shows the experimental Bode plots of the duty cycle-to-inductor current transfer function at given input voltage values. A gain of 12 dB must be added to the magnitude response to account for the duty cycle modulator gain. The resultant Bode plots are almost identical to the WF Bode plots with delay shown in Figs. 6.3(a) and 6.4.

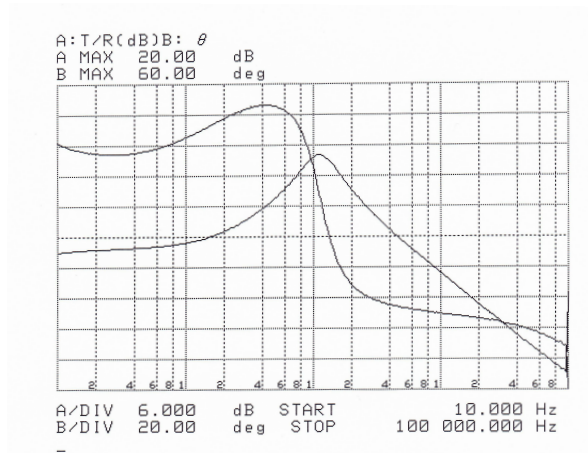
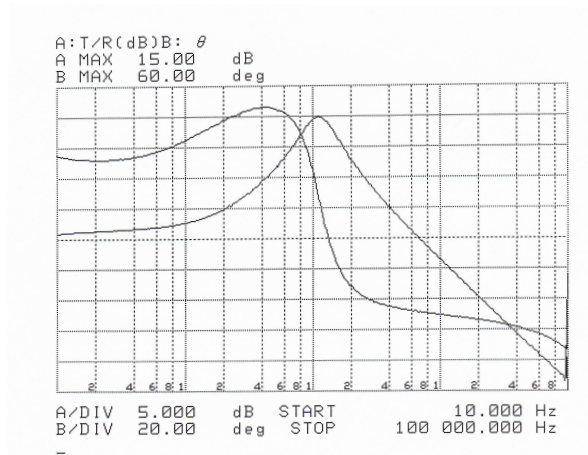
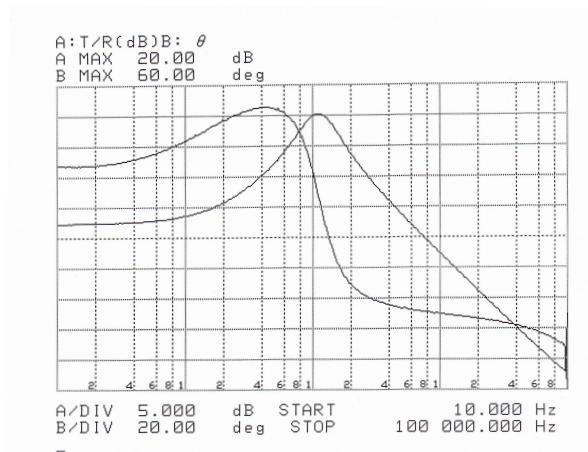
(a)  $V_I = 16$  V(b)  $V_I = 23.33$  V(c)  $V_I = 35$  V

Figure 6.5: Experimental Bode plots of duty cycle-to-inductor current transfer function from Hewlett-Packard 4194A Impedance/Gain-Phase Analyzer.



### 6.3 Duty Ratio-to-Output Voltage Transfer Function of Buck Converter

The duty cycle-to-output voltage transfer function of a dc-dc PWM buck converter in CCM, including parasitics and MOSFET delay, is derived in this section.

#### 6.3.1 Transfer Function

From Fig. 2(a),

$$v_o = i_l Z_2. \quad (6.10)$$

Therefore, the duty cycle-to-output voltage transfer function is

$$T_p(s) = \left. \frac{v_o(s)}{d(s)} \right|_{v_i=i_o=0} = \frac{V_I Z_2}{Z_1 + Z_2} = T_{px} \frac{s + \omega_z}{s^2 + 2\xi\omega_0 s + \omega_0^2}, \quad (6.11)$$

where

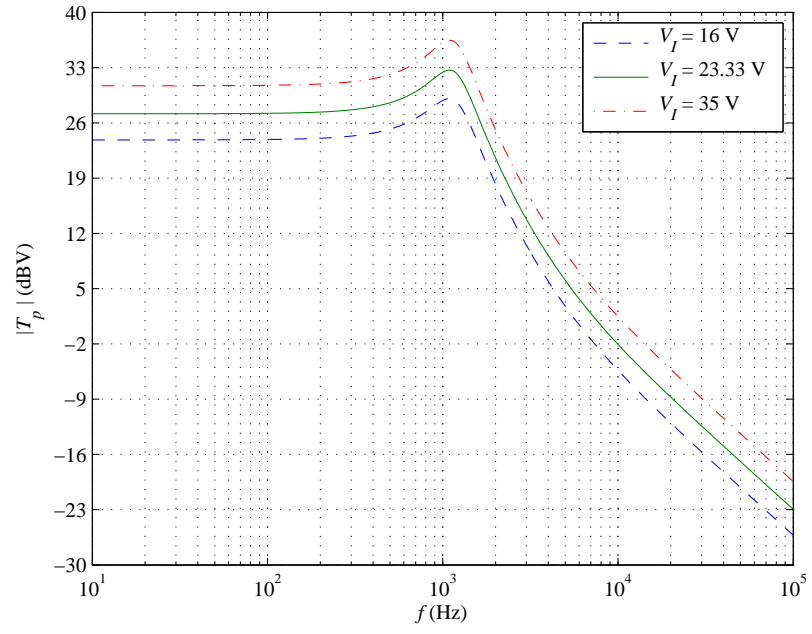
$$T_{px} = \frac{V_I R_L r_C}{L(R_L + r_C)} \text{ and } \omega_z = \frac{1}{C r_C}. \quad (6.12)$$

Including the MOSFET delay as given in (6.6), the duty ratio-to-output voltage transfer function becomes

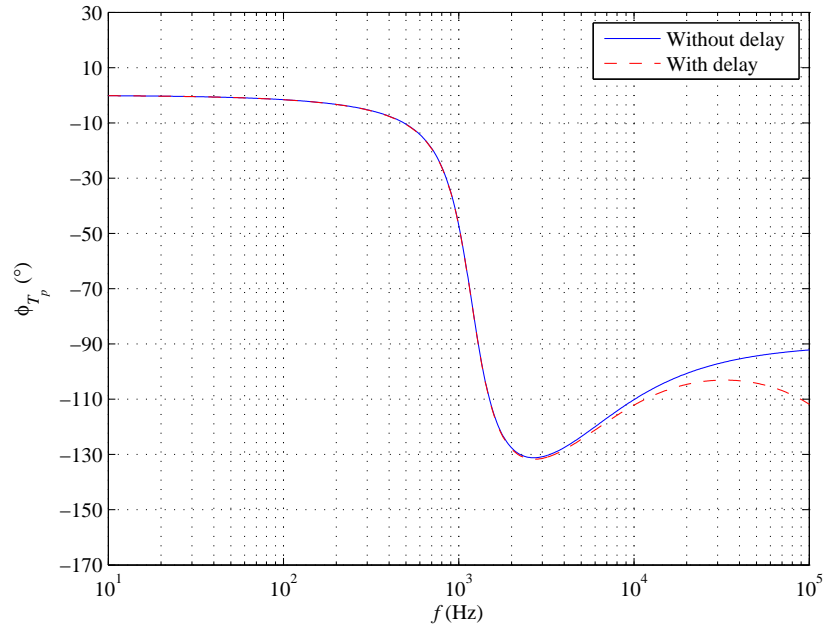
$$T_{pd}(s) = T_p(s)T_d(s) = -T_{px} \frac{s + \omega_z}{s^2 + 2\xi\omega_0 s + \omega_0^2} \frac{s - \frac{2}{t_d}}{s + \frac{2}{t_d}}. \quad (6.13)$$

#### 6.3.2 Simulation Results

Fig. 6.6 shows the Bode plots of the duty cycle-to-output voltage transfer function for the selected buck converter design at selected values of input voltage. Here also, the plots indicate that the transfer function is a low-pass filter function with one zero. The frequency of the zero is higher than that of the poles. Again, the MOSFET delay introduces additional phase at high frequencies. Table 6.2 shows the corner frequencies and the dc gain corresponding to the input frequencies.



(a)



(b)

Figure 6.6: Bode plots of duty cycle-to-output voltage transfer function at given input voltages. (a) Magnitude. (b) Phase.

Table 6.2: Corner frequencies and dc gains of  $T_p(s)$  at given values of input voltage.

$V_I$ (V)	$f_z$ (kHz)	$f_0$ (kHz)	$T_{po}$ (dBV)
16		1.1879	23.841
23.33	4.501	1.1853	27.156
35		1.183	30.707

### 6.3.3 Experimental Results

Fig. 6.7 shows the experimental Bode plots of the duty cycle-to-output voltage transfer function at specified input voltages obtained using Hewlett-Packard 4194A Gain-Phase Analyzer. A gain of 12 dB must be added to the responses to account for the duty cycle modulator gain. The resultant plots agree with the Bode plots with MOSFET delay shown in Fig. 6.6.

## 6.4 Block Diagram of Current-Mode Controlled Converters with Inner-Current Loop only

A block diagram to model the inner-current loop of peak current-mode controlled dc-dc boost converter presented in [28] is shown in Fig. 6.8(a). Let  $v_c$  and  $v_e$  be the small-signal components of the control-voltage supplied by the outer loop and the error voltage, respectively. Also,  $T_{ms}(s) = \frac{d(s)}{v_e(s)}$  is the modulator transfer function,  $T_{pi}(s) = \frac{i_l(s)}{d(s)}$  is the power stage duty cycle-to-inductor current transfer function,  $T_p(s) = \frac{v_o(s)}{d(s)}$  is the power stage duty cycle-to-output voltage transfer function,  $T_i(s) = \frac{R_s i_l(s)}{v_c(s)}$  is the loop gain of the inner loop,  $T_{icl}(s) = \frac{d(s)}{v_c(s)}$  is the closed-loop control voltage-to-duty cycle transfer function, and  $T_{co}(s) = \frac{v_o(s)}{v_c(s)}$  is the control-to-output transfer function. The control-to-output transfer function is necessary for the outer-voltage loop design as it is the plant transfer function for the outer loop.

While this block diagram can be adopted for any peak current-mode controlled non-isolated PWM dc-dc converters, it requires the power stage transfer functions and modulator transfer function to obtain the control-to-output transfer function.

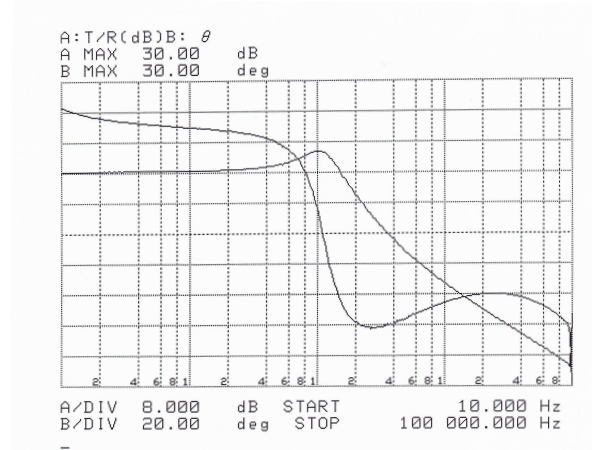
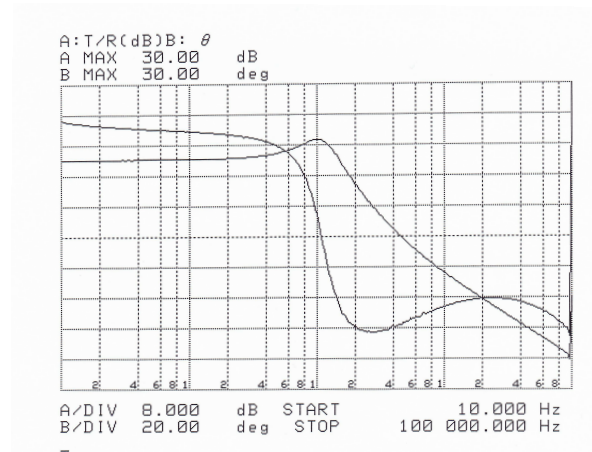
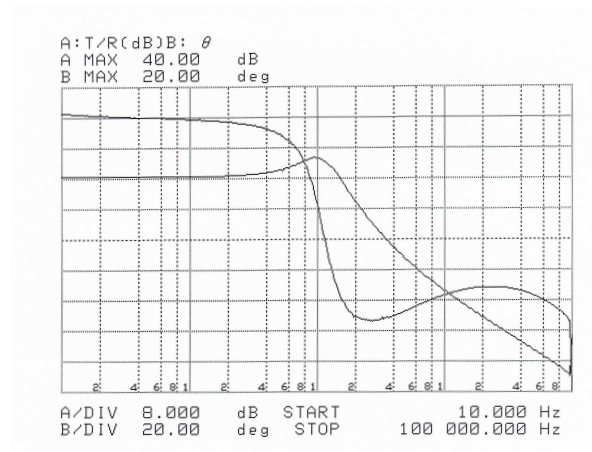
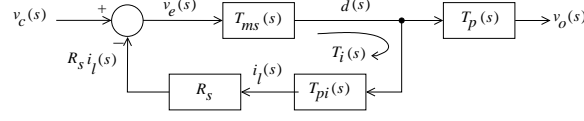
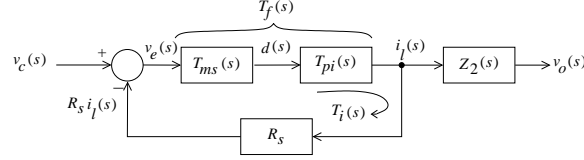
(a)  $V_I = 16$  V(b)  $V_I = 23.33$  V(c)  $V_I = 35$  V

Figure 6.7: Experimental Bode plots of duty cycle-to-output voltage transfer function from Hewlett-Packard 4194A Impedance/Gain-Phase Analyzer.



(a) Existing block diagram [28].



(b) Proposed block diagram.

Figure 6.8: Block diagrams to determine control-to-output transfer function.

For a peak current-mode controlled buck converter, as  $i_L = i_O$ , a short cut to obtain the control-to-output transfer function is to use the block diagram presented in Fig. 6.8(b). In this case, the power stage transfer functions are not required. The control-to-output transfer function is dependent only on converter independent transfer function  $H_{icl}(s)$  and the load  $Z_2(s)$ .  $H_{icl}(s) = \frac{i_l(s)}{v_c(s)}$  is the closed-loop control voltage-to-inductor current transfer function and  $Z_2(s) = \frac{v_o(s)}{i_l(s)}$  is the inductor current-to-output transfer function.

## 6.5 Closed-Loop Control-to-Inductor Current Transfer Function

The closed-loop control voltage-to-inductor current transfer function of the inner-current loop in  $s$ -domain for any PWM converter was derived in Section 2.6.3. The closed-loop gain was obtained as

$$H_{icl}(s) = \frac{i_l(s)}{v_c(s)} = \frac{1}{R_s} \frac{\omega_h^2}{s^2 + 2\xi_h \omega_h s + \omega_h^2}, \quad (6.14)$$

where the angular corner frequency and damping coefficient, respectively, are

$$\omega_h = \pi f_s \text{ and } \xi_h = \frac{\pi}{4} \frac{1-a}{1+a}. \quad (6.15)$$

As seen from (6.14), the closed-loop gain is dependent on the switching frequency and perturbation ratio. But, the inner closed-loop gain is independent of the con-

Table 6.3: Cross-over frequencies and phase margins of  $T_i(s)$  at given values of input voltage.

$V_I$ (V)	$D$	$a = \frac{D}{1-D}$	$f_{ci}/f_s$	$PM$ ( $^\circ$ )
16	0.487	0.95	0.4997	2.5
23	0.333	0.5	0.4663	29.3
35	0.23	0.289	0.4155	46.4

verter topology. Experimental results to validate the modeling were presented in Section 2.6.4.

## 6.6 Loop Gain of the Inner-Current Loop

Loop gain of the inner-current loop is necessary to analyze the relative stability of the loop. In Section 3, a general expression for loop gain was derived as

$$T_i(s) \approx \frac{\pi^2 f_s^2}{s(s + \frac{\pi^2}{2} \frac{1-a}{1+a} f_s)} = \frac{\omega_h^2}{s(s + \omega_{sh})}, \quad (6.16)$$

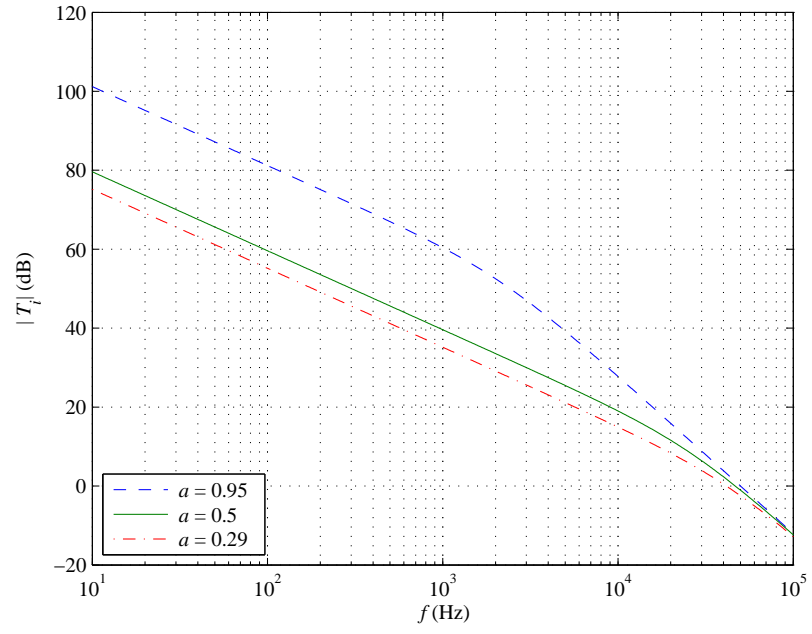
where

$$\omega_{sh} = 2\xi_h\omega_h = \frac{\pi^2}{2} \frac{1-a}{1+a} f_s. \quad (6.17)$$

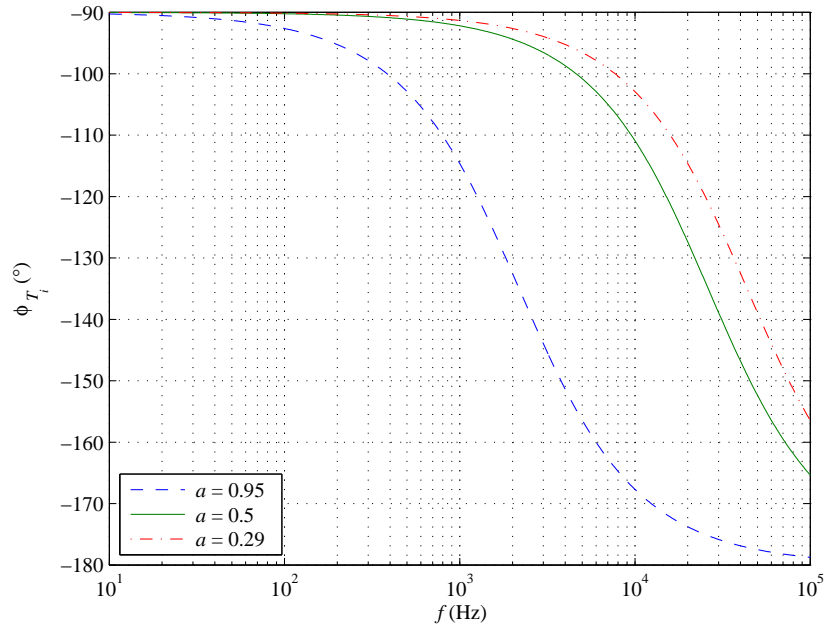
Equation (6.16) shows that the expression for loop gain of the inner-current loop is converter independent. It is only dependent on the switching frequency and the perturbation ratio. It is a second-order function with two poles, including the one at the origin.

### 6.6.1 Simulation Results

Fig. 6.9 shows the Bode plots of the loop gain with  $a = 0.29, 0.5$ , and  $0.95$  at  $f_s = 100$  kHz. The corresponding cross-over frequencies and phase margins are shown in Table 6.3. As the value of  $a$  increases, the cross-over frequency  $f_{ci}$  increases and the phase margin  $PM$  decreases. It is desirable to have low values of perturbation ratio  $a$  to have a high margin of stability.



(a)



(b)

Figure 6.9: Bode plots of loop gain  $T_i(s)$  of the inner-current loop at given values of  $a$ . (a) Magnitude. (b) Phase.

## 6.7 Error Voltage-to-Duty Cycle Transfer Function of PCM Controlled Buck Converter

The modulator transfer function or the error voltage-to-duty cycle transfer function of the inner loop is obtained as

$$\begin{aligned}
 T_{ms}(s) &= \frac{T_i(s)}{R_s T_{pi}(s)} \\
 &= \frac{\frac{\omega_h^2}{s(s+\omega_{sh})}}{R_s T_{pix} \frac{s+\omega_{zi}}{s^2+2\xi\omega_0s+\omega_0^2}} \\
 &= \frac{\omega_h^2}{R_s T_{pix}} \frac{s^2+2\xi\omega_0s+\omega_0^2}{s(s+\omega_{sh})(s+\omega_{zi})}.
 \end{aligned} \tag{6.18}$$

Fig. 6.10 illustrates the Bode plots of the modulator transfer function.

## 6.8 Control Voltage-to-Duty Cycle Transfer Function of PCM Controlled Buck Converter

The control voltage-to-duty cycle transfer function  $T_{icl}$  can be obtained as

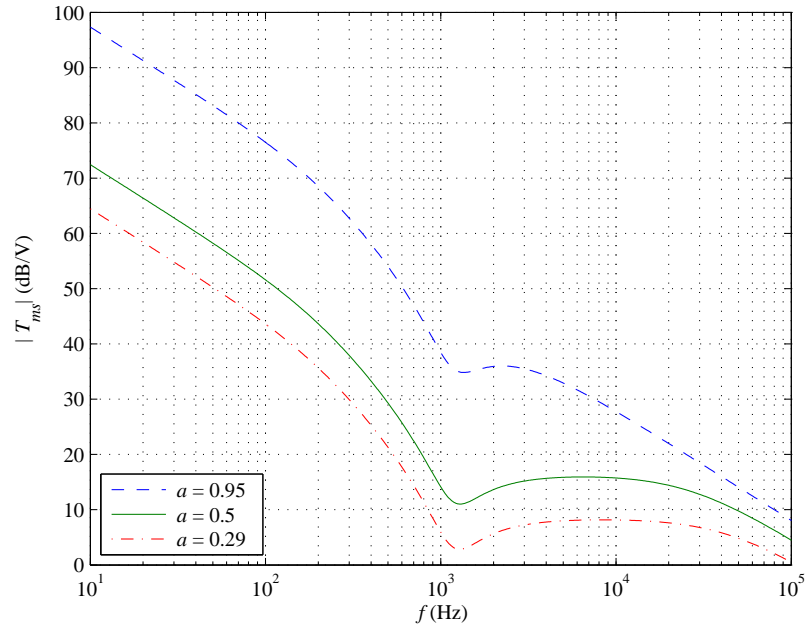
$$\begin{aligned}
 T_{icl}(s) &= \frac{T_{ms}(s)}{1+T_i(s)} \\
 &= \frac{\omega_h^2}{R_s T_{pix}} \frac{\frac{s^2+2\xi\omega_0s+\omega_0^2}{s(s+\omega_{sh})(s+\omega_{zi})}}{1+\frac{\omega_h^2}{s(s+\omega_{sh})}} \\
 &= \frac{\omega_h^2}{R_s T_{pix}} \frac{s^2+2\xi\omega_0s+\omega_0^2}{(s+\omega_{zi})(s^2+\omega_{sh}s+\omega_h^2)}.
 \end{aligned} \tag{6.19}$$

Fig. 6.11 illustrates the Bode plots of the control voltage-to-duty cycle transfer function at specified values of  $V_I$  and  $a$ .

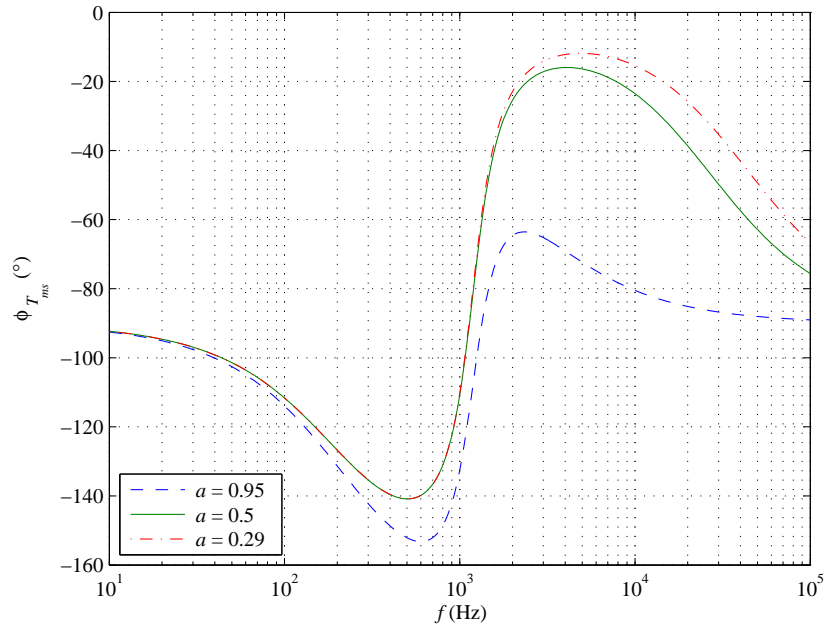
## 6.9 Control-to-Output Transfer Function of PCM Controlled Buck Converter

Control-to-output transfer function  $T_{co}(s) = \frac{v_o(s)}{v_c(s)}$  is the plant transfer function for the outer-voltage loop in a peak current-mode controlled PWM dc-dc converters. In



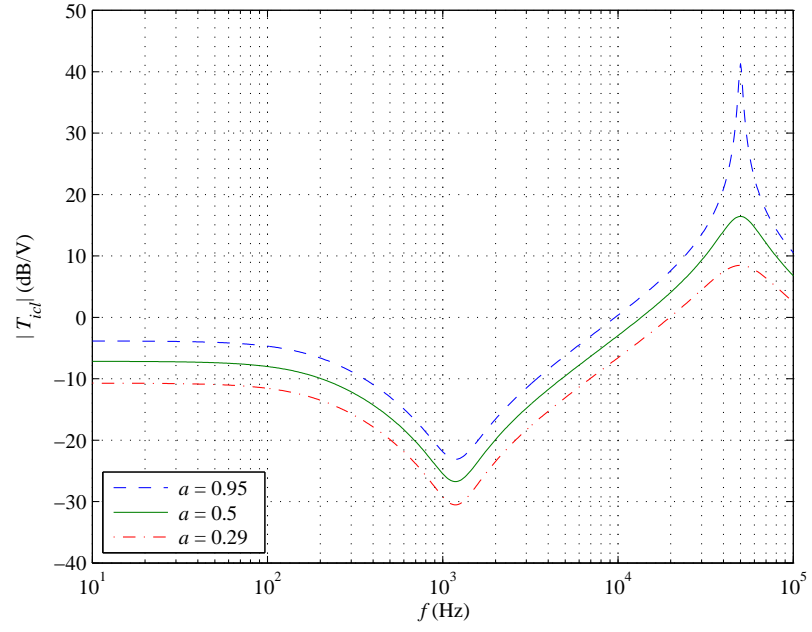


(a)

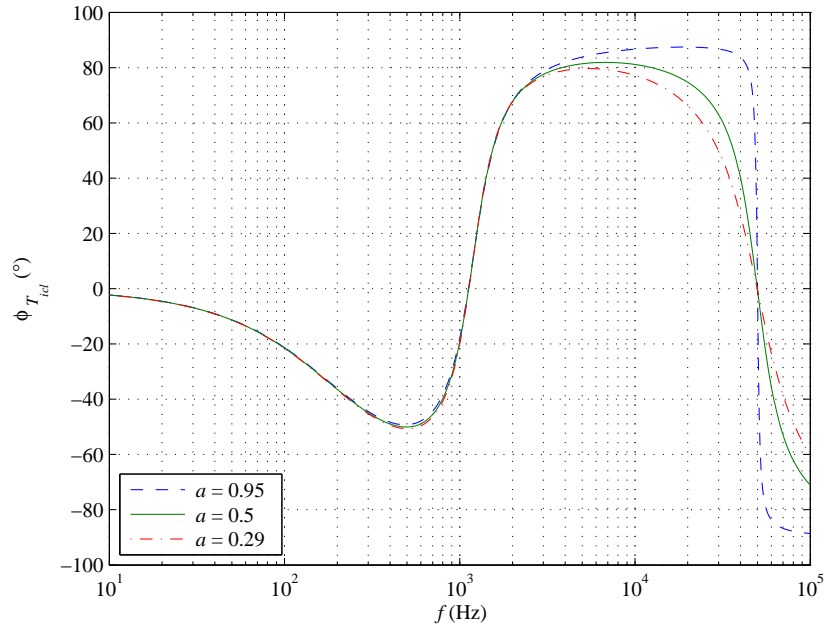


(b)

Figure 6.10: Bode plots of error voltage-to-duty cycle  $T_{ms}(s)$  transfer function at given values of  $a$ . (a) Magnitude. (b) Phase.



(a)



(b)

Figure 6.11: Bode plots of control voltage-to-duty cycle transfer function  $T_{icl}(s)$  at given values of  $a$ . (a) Magnitude. (b) Phase.

this section, the control-to-output transfer function of the inner loop of peak current-mode controlled buck converter will be derived. This transfer function is required to design the compensator in the outer-voltage loop.

### 6.9.1 Using the Existing Block Diagram

From Fig. 8(a), the control-to-output voltage transfer function is

$$\begin{aligned}
 T_{co}(s) &= \frac{v_o(s)}{v_c(s)} = \frac{d(s)}{v_c(s)} \frac{v_o(s)}{d(s)} = T_{icl}(s)T_p(s) = \frac{\frac{T_i(s)}{R_s T_{pi}(s)}}{1 + T_i(s)} T_p(s) \\
 &= \frac{T_i(s)}{1 + T_i(s)} \frac{T_{pd}(s)}{R_s T_{pid}(s)} \\
 &= \frac{\omega_h^2}{R_s T_{pix}} \frac{s^2 + 2\xi\omega_0 s + \omega_0^2}{(s + \omega_{zi})(s^2 + \omega_{sh}s + \omega_h^2)} \times T_{px} \frac{s + \omega_z}{s^2 + 2\xi\omega_0 s + \omega_0^2}, \tag{6.20}
 \end{aligned}$$

which results in

$$T_{co}(s) = \frac{R_L r_C \omega_h^2}{R_s (R_L + r_C)} \frac{s + \omega_z}{(s^2 + \omega_{sh}s + \omega_h^2)(s + \omega_{zi})}. \tag{6.21}$$

### 6.9.2 Using the Proposed Block Diagram

From Fig. 8(b), the control-to-output voltage transfer function is obtained as

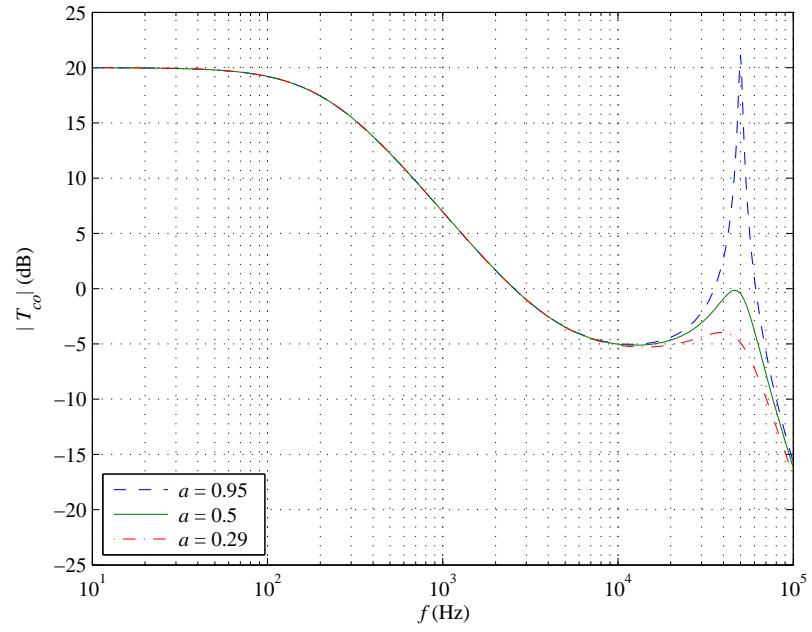
$$T_{co}(s) = \frac{v_o(s)}{v_c(s)} = \frac{i_l(s)}{v_c(s)} \frac{v_o(s)}{i_l(s)} = H_{icl}(s)Z_2(s), \tag{6.22}$$

where  $H_{icl}(s)$  is given by (6.14) and  $Z_2(s)$  is given by (6.3). Therefore, the control-to-output transfer function is obtained as

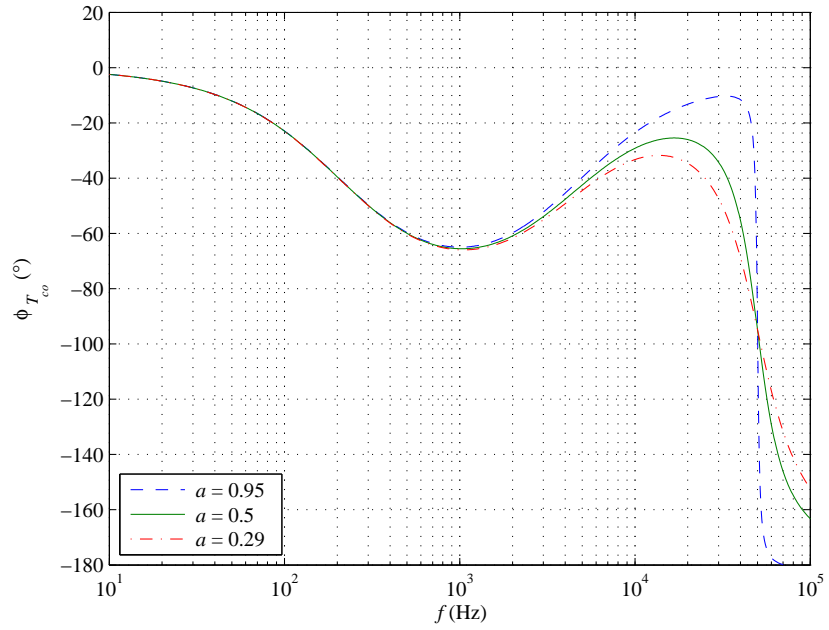
$$T_{co}(s) = \frac{R_L r_C \omega_h^2}{R_s (R_L + r_C)} \frac{s + \omega_z}{(s^2 + \omega_{sh}s + \omega_h^2)(s + \omega_{zi})}. \tag{6.23}$$

### 6.9.3 Simulation Results

Bode plots illustrating control-to-output transfer function at specified values of  $V_I$  and  $a$  are depicted in Fig. 6.12. The corresponding values of dc gain  $T_{co}(0)$ , the zero-crossing frequency  $f_{zc}$ , and the phase at zero-crossing frequency  $\phi_{T_{co}}(f_{zc})$ , which are required to design the controller for the outer loop, are shown in Table 6.4.



(a)



(b)

Figure 6.12: Bode plots of control-to-output transfer function  $T_{co}(s)$  at given values of  $a$ . (a) Magnitude. (b) Phase.

Table 6.4: Cross-over frequencies and phase values of  $T_{co}(s)$  at given values of input voltage.

$V_I$ (V)	$D$	$a = \frac{D}{1-D}$	$f_{zc}/f_s$	$\phi_{T_{co}}(f_{zc})$ ( $^\circ$ )	$T_{co}(0)$ dB
16	0.487	0.95	37	55.57	
23	0.333	0.5	27	29.3	20
35	0.23	0.289	58	46.4	

#### 6.9.4 Experimental Results

The Bode plots of control-to-output transfer function of the inner-current loop of the buck converter given in Section 2.6.4 were measured using Hewlett-Packard 4194A Impedance/Gain-Phase Analyzer. Figs. 6.13(c), 6.13(b), and 6.13(a) show the resultant Bode plots for  $a = 0.29$ ,  $a = 0.5$ , and  $a = 0.95$ , respectively. The experimental Bode plots show excellent agreement with the theoretical Bode plots shown in Fig. 6.12.

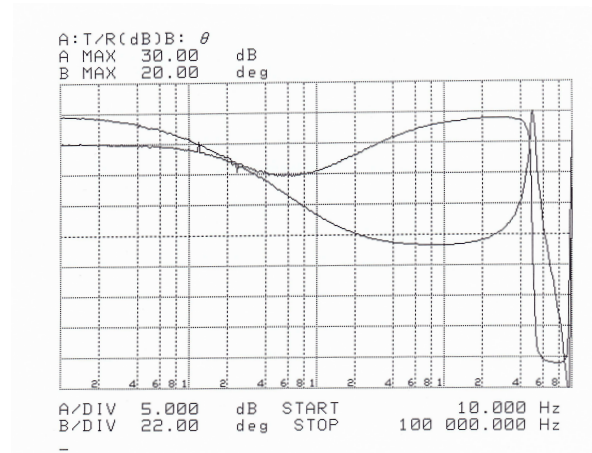
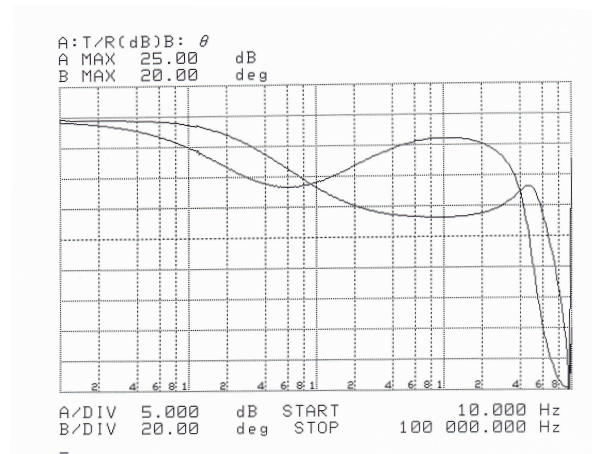
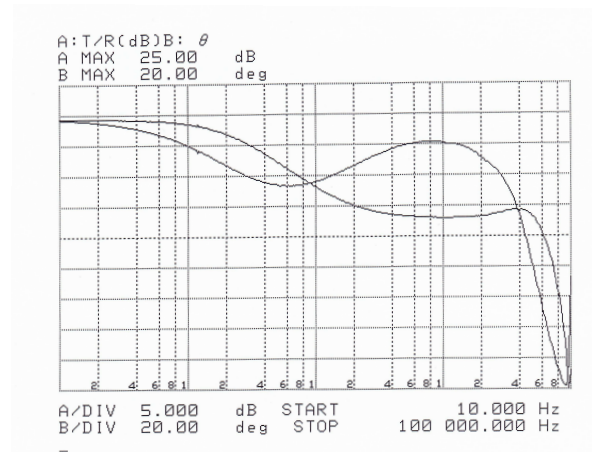
(a)  $V_I = 16$  V(b)  $V_I = 23.33$  V(c)  $V_I = 35$  V

Figure 6.13: Experimental Bode plots of control voltage-to-output voltage transfer function from Hewlett-Packard 4194A Impedance/Gain-Phase Analyzer.

## 7 Conclusions

### 7.1 Summary

The principle of operation of peak current-mode controlled PWM dc-dc converters operating in CCM has been explained. Stability of the inner-current loop has been explained using perturbation theory. Using the inner-current loop dynamics, the relationship between the small-signal control voltage and inductor current waveforms has been obtained in the  $z$ -domain. Using sample-and-hold modeling of the inner-current loop and modified Padé approximation, the closed-loop control voltage-to-inductor current transfer function has been derived in  $s$ -domain. The expression for closed-loop transfer function is independent of converter topology. Assuming a simple closed-loop structure with negative feedback, a general expression for the loop gain of peak current-mode controlled PWM dc-dc converters, independent of converter topology, has been derived. Experimental results have been presented to validate the model. From the Bode plots, the gain margin  $GM = \infty$ . An expression for phase margin  $PM$  in terms of perturbation ratio  $a$  has been derived using modified Padé approximation. It is desired to have low values of  $a$  to have a reasonable margin of stability.

For peak current-mode controlled converters without slope compensation, expressions of control current  $I_{CN}$  required to provide the specified duty cycle  $D$  for buck, boost, and buck boost converters have been derived. The relative stability of the inner loop has been analyzed. Contrary to the common belief, it was seen that slope compensation has to be employed even for  $D < 0.5$ , in order to have a reasonable margin of stability. Saber simulation results and experimental results have been presented to validate the theory.

For peak current-mode controlled converters with slope compensation, the expressions for required slope compensation to be marginally stable  $M_{3cr}$  as well as to have

a specified margin of stability  $M_{3min}$  at a given  $D_{max}$  have been derived. It was seen that  $M_{3min} = M_{3cr} + M_{3PM}$ , where  $M_{3PM}$  is a function of  $PM$ . Also, expressions for the maximum value of duty cycle that can be obtained at a given slope compensation to be marginally stable  $D_{lim}$  and to have a specified stability margin  $D_{max}$  have been derived.  $D_{max} < D_{lim}$  by a factor of  $D_{PM}$ , which is a function of  $PM$ . Expression for required control current at a given  $M_3$ ,  $D_{max}$ , and  $PM$  has been derived. Saber simulation results have been presented to validate the theory.

The dynamic behavior inner-loop has been analyzed. The power stage transfer functions  $T_p(s) = \frac{v_o(s)}{d(s)}$  and  $T_{pi}(s) = \frac{i_l(s)}{d(s)}$  are critical path transfer functions for peak current-mode controlled operation. These transfer functions have been derived for PWM dc-dc buck converter. Also, it is common belief that the power stage reduces to a current source in current-mode controlled systems. A comparison of high-frequency and wide-frequency transfer functions showed that, while this is true at high-frequencies, it does not represent the dynamic behavior of the power stage for the entire frequency range. Experimental results agreed with the wide-frequency transfer functions. Relevant inner-loop transfer functions have been derived. A reduced block diagram has been proposed to obtain the control-to-output transfer function of peak current-mode controlled PWM dc-dc buck converter in CCM. This transfer function is the plant transfer function for the outer-voltage loop and is required for the outer loop is design. The control-to-output transfer function has been derived and has been validated using experimental results.

## 7.2 Contributions

The contributions of this dissertation are:

- General expression for loop gain  $T_i(s)$  of the inner-current loop of peak current-mode controlled PWM dc-dc converters was derived using modified Padé approximation.



- For peak current-mode controlled converters without slope compensation:
  - Relationship between relative stability of the inner loop in terms of phase margin and duty cycle.
  - Expression for the control current  $I_{CN}$  required by the current loop.
- For peak current-mode controlled converters with slope compensation:
  - Expression for critical value of compensation slope  $M_{3cr}$  required to obtain the given maximum duty cycle  $D_{max}$  for a marginally stable loop.
  - Expression for limiting value of duty cycle  $D_{lim}$  that can be obtained at a given slope compensation  $M_3$  for a marginally stable loop.
  - Expression for minimum value of compensation slope  $M_{3min}$  required at a given maximum duty cycle  $D_{max}$  and phase margin  $PM$ .
  - Expression for maximum duty cycle  $D_{max}$  that can be obtained at a given slope compensation  $M_3$  and phase margin  $PM$ .
  - Expression for control current  $I_{CS}$  required by the inner-current loop.
- Derivation of power stage transfer functions  $T_{pi}(s)$  and  $T_p(s)$  in the critical path of peak current-mode controlled PWM dc-dc buck converter.
- Block diagram to represent the inner loop of peak current-mode controlled PWM dc-dc buck converter.
- Control-to-output transfer function  $T_{co}(s)$  for peak current-mode controlled PWM dc-dc buck converter.

## References

- [1] C. W. Deisch, "Switching control method changes power converter into a current source," in *PESC'78; IEEE Power Electron. Spec. Conf. Record*, 1978, pp. 300–306.
- [2] S. P. Hsu, A. Brown, L. Rensink, and R. D. Middlebrook, "Modelling and analysis of switching dc-to-dc converters in constant-frequency current programmed mode," in *PESC'79; IEEE Power Electron. Spec. Conf. Record*, 1979, pp. 284–301.
- [3] A. R. Brown and R. D. Middlebrook, "Sampled-data modeling of switching regulators," in *PESC'81; IEEE Power Electron. Spec. Conf. Record*, 1981, pp. 349–369.
- [4] B. H. Cho and F. C. Lee, "Measurement of loop gain with the digital modulator," in *PESC'84; IEEE Power Electron. Spec. Conf. Record*, 1984, pp. 363–373.
- [5] R. Redl and N. O. Sokal., "Current-mode control, five different types, used with three basic classes of power converters: Small-signal ac and dc characterization, stability requirements, and implementation of practical circuits," in *PESC'85; IEEE Power Electron. Spec. Conf. Record*, 1985, pp. 771–785.
- [6] D. M. Mitchell, "An analytical investigation of current-injected control for constant-frequency switching regulators," *IEEE Trans. Power Electron.*, vol. PE-1, no. 3, pp. 167–174, 1986.
- [7] R. D. Middlebrook, "Topics in multiple-loop regulators and current-mode programming," *IEEE Trans. Power Electron.*, vol. PE-2, no. 2, pp. 109–124, April 1987.
- [8] G. K. Schoneman and D. M. Mitchell, "Closed-loop performance comparisons of switching regulators with current-injected control," *IEEE Trans. Power Electron.*, vol. 3, no. 1, pp. 31–43, 1988.
- [9] ———, "Output impedance considerations for switching regulators with current-injected control," *IEEE Trans. Power Electron.*, vol. 4, no. 1, pp. 25–35, 1989.
- [10] G. Verghese, C. Bruzos, and K. Mahabir, "Averaged and sampled-data models for current mode control," in *IEEE Power Electron. Spec. Conf. Record*, 1989, pp. 484–491.
- [11] R. D. Middlebrook, "Modeling current-programmed buck and boost regulators," *IEEE Trans. Power Electron.*, vol. 4, no. 1, pp. 36–52, January 1990.
- [12] R. B. Ridley, "A new, continuous-time model for current-mode control," *IEEE Trans. Power Electron.*, vol. 6, no. 2, pp. 271–280, April 1991.
- [13] R. Redl, "High-frequency expansion of the small-signal model of the constant frequency current-mode controlled converters," in *Proc. APEC*, 1991, pp. 466–472.
- [14] A. Kislovski, "Current-mode control: A unified model for open-loop instability," in *Proc. APEC*, 1991, pp. 459–465.

- [15] A. V. Anunciada and M. M. Silva, "A new current mode control process and applications," *IEEE Trans. Power Electron.*, vol. 6, pp. 601–610, October 1991.
- [16] W. Tang, F. C. Lee, and R. B. Ridley, "Small-signal modelling of average current-mode control," *IEEE Trans. Power Electron.*, vol. 8, no. 2, pp. 112–119, April 1993.
- [17] D. Czarkowski and M. K. Kazimierczuk, "Energy-conservation approach to modeling pwm dc-dc converters," *IEEE Trans. Aerospace Electron. Syst.*, vol. AES-29, pp. 1059–1063, July 1993.
- [18] R. Tymerski and D. Li, "State-space models for current programmed pulsewidth modulated converters," *IEEE Trans. Power Electron.*, vol. 8, pp. 271–278, July 1993.
- [19] F. D. Tan and R. D. Middlebrook, "A unified model for current-programmed converters," *IEEE Trans. Power Electron.*, vol. 10, no. 4, pp. 397–408, July 1995.
- [20] K. Smidley and S. Čuk, "One-cycle control of switching converters," *IEEE Trans. Power Electron.*, vol. 10, no. 6, pp. 625–633, November 1995.
- [21] J. P. Gegner and C. Q. Lee, "Linear peak current mode control: a simple active power factor correction control technique for continuous conduction mode," in *PESC'96, IEEE Power Electron. Spec. Conf. Record*, vol. 1, 1996.
- [22] B. Choi, "Step load response of a current-mode-controlled dc-to-dc converter," *IEEE Trans. Aerospace and Electron. Syst.*, vol. 33, no. 4, pp. 1115–1121, October 1997.
- [23] Y.-W. Lo and R. J. King, "Sampled-data modeling of the average-input current-mode controlled buck converter," *IEEE Trans. on Power Electron.*, vol. 14, no. 5, pp. 918–927, September 1999.
- [24] M. K. Kazimierczuk, "Transfer function of current modulator in pwm converters with current-mode control," *IEEE Trans. Circuits and Systems I*, vol. 47, no. 9, pp. 1407–1412, September 2000.
- [25] P. Midya, P. T. Krein, and M. F. Greuel, "Sensorless current mode control - an observer-based technique for dc-dc converters," *IEEE Trans. on Power Electron.*, vol. 16, no. 4, pp. 522–526, July 2001.
- [26] B. Bryant and M. Kazimierczuk, "Sample and hold effect in PWM DC-DC converters with peak current-mode control," in *IEEE Intern. Symp. on Circ. and Syst.; ISCAS'04*, vol. 5, 2004.
- [27] B. Choi and W. Lim, "Current-mode control to enhance closed-loop performance of asymmetrical half-bridge DC-DC converters," *IEE Proceedings-Electric Power Applications*, vol. 152, no. 2, pp. 416–422, 2005.
- [28] B. Bryant and M. K. Kazimierczuk, "Modeling the closed-current loop of pwm boost dc-dc converters operating in ccm with peak current-mode control," *IEEE Trans. Circuits Syst.*, vol. 52, no. 11, pp. 2404–2412, November 2005.
- [29] —, "Voltage-loop of boost dc-dc converters with peak current-mode control," *IEEE Trans. Circuits Syst.*, vol. 53, no. 1, pp. 99–105, January 2006.

- [30] S. Chattopadhyay and S. Das, "A digital current-mode control technique for dc-dc converters," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1718–1726, November 2006.
- [31] R. Sheehan, "A new way to model current-mode control," *Power Electronics Technology I*, pp. 14–20, May 2007.
- [32] —, "A new way to model current-mode control," *Power Electronics Technology II*, pp. 22–32, June 2007.
- [33] M. K. Kazimierczuk, *Pulse-Width Modulated DC-DC Power Converters*, 1st ed. John Wiley & Sons, 2008.
- [34] N. Kondrath and M. K. Kazimierczuk, "Margins of stability of inner-current loop of peak current-mode controlled pwm dc-dc converters," in *IEEE International Symposium on Circuits and Syst.*, 2009, pp. 1985–1988.
- [35] S. Cuk, "General topological properties of switching structures," in *PESC'79; IEEE Power Electron. Spec. Conf. Record*, 1979, pp. 109–130.
- [36] B. Lau and R. Middlebrook, "Small-signal frequency response theory for piecewise-constant two-switched-network dc-dc converter system," in *PESC'86; IEEE Power Electron. Spec. Conf. Record*, 1986, pp. 186–200.
- [37] V. Vorperian, "Simplified analysis of PWM converters using model of PWM switch. I, Continuous conduction mode," *IEEE Trans on Aerospace and Electron. Syst.*, vol. 26, no. 3, pp. 490–496, 1990.
- [38] M. K. Kazimierczuk and D. Czarkowski, "Application of the principle of energy conservation to modelling the pwm converters," in 2nd IEEE Conf. on Control Applications, September 13–16, 1993, pp. 291–296.
- [39] S. Ben-Yaakov and D. Edry, "Averaged models as tools for studying the dynamics of switch mode dc-dc converters," in *PESC'94; IEEE Power Electron. Spec. Conf. Record*, 1994, pp. 1218–1225.
- [40] B. Bryant and M. K. Kazimierczuk, "Open-loop power-stage transfer functions relevant to current-mode control of boost pwm converter operating in ccm," *IEEE Trans. Circuits Syst.*, vol. 52, no. 10, pp. 2158–2164, October 2005.
- [41] —, "Voltage-loop power-stage transfer functions with mosfet delay for boost pwm converter operating in ccm," *IEEE Trans. Industrial Electron.*, vol. 54, no. 2, pp. 347–353, February 2007.
- [42] N. Das and M. K. Kazimierczuk, "An overview of technical challenges in the design of current transformers," in *Electrical Insulation Conference and Electrical Manufacturing Expo*, 2005, pp. 369–377.
- [43] N. Kondrath and M. K. Kazimierczuk, "Bandwidth of current transformers," *IEEE Transactions on Instrumentation and Measurements*, vol. 58, no. 6, pp. 2008–2016, June 2009.